REMARKS

Applicants have amended their claims in order to further clarify the definition of various aspects of the present invention. Specifically, Applicants have amended claim 1 to recite a plurality of memory cells; to recite that a plurality of first electrodes are formed respectively for the capacitor elements over the gate electrodes of the respective MISFETs; to recite that the dielectric film is deposited on the plurality of first electrodes; to recite that a mask layer has a predetermined pattern larger than each of the plurality of first electrodes; and to recite that both the conductive film and the dielectric film are etched in order to form second electrodes for the plurality of capacitor elements, with the second electrodes being formed in order to be connected as second electrodes of the capacitor elements of the plurality of memory cells. Claim 1, as amended, deletes recitation that the etching also etches the dielectric film over the other of the source and drain regions of the MISFET. Claim 2 has been amended in light of amendments to claim 1.

Claim 4 has been amended to recite that the device produced has a plurality of MISFETs and a plurality of capacitor elements. Claim 4 has been further amended to recite that the first conductive film is patterned in order to form a plurality of first electrodes for the plurality of capacitor elements, with each of the plurality of first electrodes extending respectively over gate electrodes of the plurality of MISFETs; to recite that the dielectric film is deposited on the plurality of first electrodes; to recite that the second conductive film and the dielectric film are etched in order to form second electrodes for the plurality of capacitor elements; and to recite that the patterned dielectric film has substantially a same pattern as that of the second electrodes and

exists only under the second electrodes, with this patterned dielectric film not extending over the other of the source and drain regions of the respective one of the plurality of MISFETs, and wherein the second electrode is larger than the plurality of first electrodes in the first and second directions and is formed in order to cover at least each of the one of the source region and the drain region of the plurality of MISFETs.

Claim 5 has been amended to recite that the semiconductor integrated circuit device produced has a plurality of MISFETs and a plurality of capacitor elements; to recite that a plurality of first electrodes for the capacitor elements are formed over the semiconductor substrates, with each of the plurality of first electrodes respectively extending over gate electrodes of the plurality of MISFETs; to recite that a dielectric film is deposited on the plurality of first electrodes; to recite that the conductive film and dielectric film are patterned respectively to form second electrodes and a patterned dielectric film; and to recite that the patterned dielectric film has substantially a same pattern as that of the second electrodes, with the patterned dielectric film not extending over the other of the source and drain regions of each of the plurality of MISFETs, and wherein the second electrodes are larger than the plurality of first electrodes and are formed in order to cover at least each gate electrode of the plurality of MISFETs. Claims 6 and 7 have been amended in light of amendments to claim 5.

In addition, Applicants are adding new claims 8-14 to the application. All of these newly added claims are directed to a method of producing a semiconductor integrated circuit device, with claim 8 being the sole newly added independent claim. Claim 8 defines a method of producing such device having word lines, data lines and a plurality of memory cells each connected to one of the word and data lines, each of the plurality

of memory cells having a MISFET and a capacitor element. The method recited in claim 8 includes steps of forming a plurality of first electrodes for the capacitor elements over the gate electrodes of the MISFETs, each of the plurality of first electrodes being electrically connected to one of the source region and drain region of a respective MISFET and extending over the gate electrode thereof; depositing dielectric and conductive films respectively on the plurality of first electrodes and on the dielectric film; forming a mask layer having a predetermined pattern larger than each of the plurality of first electrodes in directions which the data and word lines extend, over the conductive film; and etching the conductive and dielectric films to form second electrodes for the plurality of capacitor elements, with this etching also etching the dielectric film over the other of the source and drain regions of the MISFETs, and wherein the second electrodes are formed in order to be connected as second electrodes of the capacitor elements of the plurality of memory cells. Claims 9 and 10, each dependent on claim 8, respectively recites that after the etching, the dielectric film exists only under the second electrodes; and recites that the dielectric film has at least a double-layer structure of a silicon nitride film and a silicon oxide film stacked on the silicon nitride film. Claims 11 and 13, dependent respectively on claims 8 and 1, recite that each of the second electrodes is formed so as to be connected as second electrodes of more than one capacitor element; and claims 12 and 14, dependent respectively on claims 11 and 13, recite that these second electrodes are formed so as to be connected as second electrodes of capacitor elements of adjacent memory cells.

In connection with the newly added claims, as well as amendments to previously considered claims, note, for example, pages 42, 43 and 78-89 of Applicants' specification.

The obviousness-type double patenting rejection of claims 1-7 over claims 1-21 of U.S. Patent No. 6,281,071, is noted. In connection therewith, the Examiner has indicated that a timely filed Terminal Disclaimer may be used to overcome the double patenting rejection.

However, it is respectfully submitted that a Terminal Disclaimer, with respect to U.S. Patent No. 6,281,071, has already been filed in the above-identified application, on December 3, 2001, when originally filing the above-identified application. In connection therewith, note the enclosed postcard receipt in connection with the papers filed on December 3, 2001, when initially filing the above-identified application. This postcard receipt indicates that a Terminal Disclaimer, as well as the necessary fee, were filed with the original application papers. If the Examiner needs another copy of this Terminal Disclaimer, the Examiner is respectfully requested to contact the undersigned, for a copy thereof. In view of the prior filing of this Terminal Disclaimer, with respect to U.S. Patent No. 6,281,071, clearly the obviousness-type double patenting rejection is improper and must be withdrawn.

Contentions made by the Examiner on page 2 of the Office Action mailed January 24, 2003, in connection with the obviousness-type double patenting rejection, are noted. In view of the prior filing of the Terminal Disclaimer, as discussed previously, no discussion of the merits of the obviousness-type double patenting rejection is necessary. Suffice it to say that the Terminal Disclaimer was previously submitted in

order to facilitate proceedings in connection with the above-identified application, so as to achieve earliest possible issuance of a U.S. patent based thereon; and that the filing of the Terminal Disclaimer, particularly previously filed, does not constitute an admission as to the propriety of, or agreement with, the obviousness-type double patenting rejection; and does not constitute an admission as to the propriety of, or agreement with, arguments made by the Examiner in connection with the obviousness-type double patenting rejection.

Applicants respectfully submit that all of the claims presented for consideration by the Examiner patentably distinguish over the teachings of the references applied by the Examiner in rejecting claims in the Office Action mailed January 24, 2003, that is, the teachings of the U.S. patents to Moriuchi, et al., No. 4,882,289, to Kuesters, No. 4,855,801, to Takemae, et al., No. 4,649,406, and to Kimura, et al., No. 4,742,018, under the provisions of 35 USC 103.

Initially, it is stated by the undersigned that the above-identified application and Moriuchi, et al. are commonly owned (that is, by Hitachi, Ltd.). Moreover, noting that Moriuchi, et al. has a publication date of November 21, 1989 and a filing date of April 22, 1988, Moriuchi, et al. only qualifies as prior art under 35 USC 102(e). However, since the above-identified application has an actual filing date of December 3, 2001, it is respectfully submitted that Moriuchi, et al. is disqualified as prior art under 35 USC 103, based upon presently amended 35 USC 103. For this reason alone, it is respectfully submitted that a rejection on Moriuchi, et al. must fail.

In addition, the filing date of Moriuchi, et al., that is, April 22, 1988, is again noted. This date of April 22, 1988 is after the filing dates of the Japanese Patent

Applications upon which the above-identified application claims priority under 35 USC 119. Priority based upon each of seven (7) Japanese patent applications was claimed in the above-identified application, in, for example, the Claim for Priority filed December 3, 2001, in the above-identified application. It was indicated in this Claim for Priority that certified copies of each of the listed Japanese Patent Applications were filed on September 19, 1988, in prior Application No. 07/246,514, filed September 19, 1988. It is respectfully requested that the Examiner acknowledge the Claim for Priority under 35 USC 119 in the above-identified application, and indicate that all of the certified copies were previously received, in Application No. 07/246,514.

In addition, enclosed herewith please find an English translation of Japanese Patent Application No. 62-235913, filed on September 19, 1987 (one of the applications upon which a Claim for Priority under 35 USC 119 is based in the present application), with Declaration indicating accuracy of the translation. This English translation has previously been filed in Application No. 09/317,999, filed May 25, 1999, which has issued as U.S. Patent No. 6,281,071, the English translation having been submitted with the Amendment filed March 13, 2001 in No. 09/317,999. As can be seen in this English translation, and particularly on pages 23, 24 and 60-69 thereof, Japanese Patent Application No. 62-235913 clearly supports the presently claimed subject matter within the meaning of the first paragraph of 35 USC 112; moreover, as seen, for example, in the claims on pages 1-4 of this English translation, No. 62-235913 is directed to the same invention as in the above-identified application.

In view of all of the foregoing, it is respectfully submitted that Applicants have satisfied all procedural and substantive requirements of 35 USC 119 and 37 CFR 1.55,

so as to be accorded benefit of the filing date of Japanese Patent Application No. 62-235913, filed September 19, 1987. Accordingly, clearly Moriuchi, et al. does not constitute prior art in connection with the above-identified application, and for this reason also the prior art rejection based on Moriuchi, et al. must be withdrawn.

Furthermore, note that the applied reference to Kimura, et al. has a patent date of May 3, 1988, which is after the filing date of Japanese Patent Application No. 62-235913, discussed previously. Thus, Kimura, et al. only qualifies as prior art under 35 USC 102(e), based upon a filing date of December 1, 1986 for the application issuing as Kimura, et al. However, note that the above-identified application and Kimura, et al. have identical assignees, that is, Hitachi, Ltd. In view thereof, and again noting the actual filing date of the above-identified application of December 3, 2001, it is respectfully submitted that Kimura, et al. is disqualified as prior art in connection with the above-identified application. For this reason alone, it is respectfully submitted that the rejection based on Kimura, et al. must be withdrawn.

In any event, it is respectfully submitted that proper (that is, non-disqualified) prior art as applied by the Examiner would have neither taught nor would have suggested the method of producing a semiconductor integrated circuit device as in the present claims. Specifically, with respect to claim 1, it is respectfully submitted that the applied prior art would have neither taught nor would have suggested such method of fabricating the device having the recited structure of the plurality of memory cells which each include a MISFET and capacitor element, and wherein a conductive film is deposited on a dielectric film, a mask layer having a specified predetermined pattern is formed over the conductive film, and then both the conductive film and the dielectric film

are etched at a portion exposed from the mask layer in order to form second electrodes for the plurality of capacitor elements, with the second electrodes being formed in order to be connected as second electrodes of the capacitor elements of the plurality of memory cells.

In addition, it is respectfully submitted that the proper prior art applied by the Examiner would have neither disclosed nor would have suggested such method for forming the specified structure including the plurality of MISFETs and the plurality of capacitor elements each having a first electrode respectively connected to one of the source region and the drain region of a respective one of the plurality of MISFETs, including, inter alia, depositing a dielectric film on the plurality of first electrodes of the capacitor elements and depositing a second conductive film on the dielectric film, with the second conductive film and the dielectric film being etched in order to form second electrodes for the plurality of capacitor elements and a patterned dielectric film, the patterned dielectric film having substantially a same pattern as that of the second electrodes and existing only under the second electrodes, the patterned dielectric film not extending over the other of the source and drain regions of the plurality of MISFETs, and wherein the second electrodes are larger than the plurality of first electrodes in the first and second directions and are formed in order to cover at least each of one of the source and drain regions of the plurality of MISFETs. See claim 4; note also claim 2.

Moreover, it is respectfully submitted that the applied proper prior art would have neither taught nor would have suggested such method of producing a semiconductor integrated circuit device having the structure as recited in the present claims, including steps of depositing a dielectric film on the plurality of first electrodes of the capacitor

elements and depositing a conductive film on the dielectric film; and patterning the conductive and dielectric films respectively to form second electrodes and a patterned dielectric film, the patterned dielectric film having substantially a same pattern as that of the second electrodes, the patterned dielectric film not extending over the other of the source and drain regions of each of the plurality of MISFETs, and the second electrode being larger than the plurality of first electrodes in the first and second directions and being formed in order to cover at least each gate electrode of the plurality of MISFETs. See claim 5.

Furthermore, it is respectfully submitted that the applied proper prior art would have neither taught nor would have suggested such method of producing a semiconductor integrated circuit device as in the present claims, having the recited structure, the process including depositing a dielectric film and a conductive film respectively on the plurality of first electrodes and on the dielectric film; forming a mask layer having a predetermined pattern larger than each of the plurality of first electrodes in directions which the data and word lines extend, over the conductive film; and etching both the conductive and dielectric films at a portion exposed from the mask layer in order to form second electrodes for the plurality of capacitor elements, the etching procedure also etching the dielectric film over the other of the source and drain regions of the MISFETs, and the second electrodes being formed in order to be connected as second electrodes of the capacitor elements of the plurality of memory cells. See claim 8.

The applied proper prior art would not have disclosed or suggested the aspects of the present invention in the remaining, dependent claims, having features as

discussed previously, and further (but not limited to) wherein the second electrodes are connected so as to be second electrodes for a plurality of capacitor elements of the memory cells (see claims 11 and 13); in particular, adjacent memory cells (see claims 12 and 14).

The present invention is directed to a method of forming a semiconductor integrated circuit device, particularly a semiconductor integrated circuit memory device such as a DRAM having a stacked capacitor element. In particular, the present invention addresses problems arising upon increasing integration densities of the DRAM.

Upon increasing integration density of the DRAM, the memory cell is required to have an isolating space between the first electrode layer of the stacked capacitor element and an intermediate conducting layer which connects a data line to a semiconductor region of the memory cell selecting MISFET. Such isolating space causes a decrease in the area of the first electrode layer of the stacked capacitor element, and, accordingly, decreases amount of storage of electrical charges which can be achieved in the stacked capacitor element. Moreover, when the second electrode layer of the stacked capacitor element is to be patterned, the intermediate conducting layer uses a dielectric film formed thereover as an etching stopper; however, this dielectric film is very thin, and can be damaged or broken as a result of over-etching in patterning the second electrode layer, causing a poor connection between the data line and the other semiconductor region of the MISFET.

Against this background, Applicants provide a method wherein integration density of the DRAM can be increased without deteriorating reliability of the DRAM,

while still satisfactorily providing the stacked capacitor element and data line connection to the other semiconductor region of the memory cell selecting MISFET. Applicants have found that by providing the second electrode having a larger pattern than the first electrode in both word line and data line directions, and by etching both the second electrode and dielectric film with a same mask or by utilizing the second electrode as a mask in etching the dielectric film, objectives according to the present invention are achieved. That is, by utilizing the second electrode layer according to the present invention, electrical charges stored in the dielectric film at the time of plasma etching to form the second electrode layer or in later processing steps can be reduced, so that the insulating breakdown voltage of the dielectric film can be improved. As a result, it is possible to improve electrical reliability of the DRAM. Moreover, the inter-layer insulating film can be removed from the semiconductor region which is to be connected with the data line by using the second electrode layer or its patterning mask as a mask in removing the inter-layer insulating film, so that the number of steps in fabricating the DRAM can be reduced. Note pages 22 and 23 of Applicants' specification.

In addition, according to the present invention, the electrodes of the information storing capacitor of a plurality of memory cells can be connected to a power source voltage of $1/2V_{cc}$; and the second electrode layer can be made integral with the second electrode layer of the information storing capacitor of another memory cell adjoining the corresponding memory cell.

Kuesters discloses a transistor varactor structure for a dynamic semiconductor storage means formed on a doped silicon substrate. The arrangement is described

most generally at column 2, lines 49-63, and a technique for forming the arrangement is described, inter alia, in column 4 and shown in Figs. 4 and 5.

As is particularly clear in Fig. 5 of Kuesters, dielectric layer D1 extends beyond upper doped polysilicon layer P2. It is respectfully submitted that this patent would have neither taught nor would have suggested, and in fact would have taught away from, the presently claimed method, including the etching or the structure formed.

Kimura, et al. discloses a process for producing a charge storage capacitor for a DRAM which is minute and yet has a large capacity, the process being described most generally in column 2, lines 12-29. See also column 2, lines 29-35. This patent discloses use of high-temperature heat treatment carried out in an oxidizing atmosphere to grow a second insulator 31 (see Fig. 2F) which defines a dielectric or a capacitor on the whole surfaces of the polycrystalline silicon layers 28 and 30.

It is emphasized that Kimura, et al. discloses a dielectric grown by thermal oxidation. Even assuming, arguendo, that Kimura, et al. qualifies as prior art under 35 USC 103 (note prior arguments that this reference is disqualified as prior art), it is respectfully submitted that the teachings of this patent would not have disclosed nor would have suggested depositing a dielectric film. Moreover, it is respectfully submitted that this patent would have neither taught nor would have suggested the etching or removing steps, or use of the mask as in the present claims, or patterns formed for the capacitor element components.

Takemae, et al. discloses metal-oxide dynamic semiconductor memory devices having stacked capacitor-type memory cells, the device arrangement being described most generally in column 1, lines 52-60. Note also column 3, lines 48-55 of this patent.

See Fig. 4 and the description at, for example, column 4, lines 44-57, describing formation of specific structure of this arrangement. Note also column 5, lines 17-48.

It is respectfully submitted that Takemae, et al. does not disclose a process to provide structure of a second electrode having a larger pattern than a first electrode in word and data line directions. Moreover, in various embodiments, Takemae, et al. shows etching the second electrode, dielectric film and first electrode using a resist pattern as a mask. See column 5, lines 49-60 of Takemae, et al. It is respectfully submitted that this patent would have neither taught nor would have suggested the method according to the present invention, or advantages achieved thereby.

Attention is respectfully directed to the enclosed "APPENDIX", showing structure formed in Takemae, et al., where each of the first and second capacitor electrodes and dielectric are etched using a single mask; and the present invention, using a single mask to etch the second electrode and dielectric (but not the first electrode). As is clear in the Appendix, in the structure in Takemae, et al., undesirable leakage current occurs. It is respectfully submitted that Takemae, et al. would have neither taught nor would have suggested the present invention, and advantages achieved thereby.

Furthermore, it is respectfully submitted that none of the applied proper prior art would have disclosed or suggested that feature according to the present invention wherein the second electrode can be formed in order to connect with a plurality of memory cells. Note especially claims 11-14.

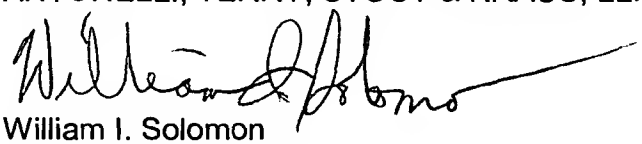
In view of the foregoing comments and amendments, reconsideration and allowance of all claims remaining in the application are respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The changes are shown on the attachment captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.262447) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims presently in the application as follows:

1. (Amended) A method of producing a semiconductor integrated circuit device having word lines, data lines and a plurality of memory cells each connected to one of the word lines and one of the data lines, each of said plurality of memory cells ~~each~~ having (1) a MISFET having a gate electrode and a source region and a drain region on a semiconductor substrate and (2) a capacitor element connected in series, comprising the steps of:

(a) forming a plurality of first ~~electrode~~electrodes respectively for ~~said~~the capacitor ~~element~~elements over ~~said~~the gate ~~electrode~~electrodes of ~~said~~ ~~MISFET~~respective MISFETs, said first ~~electrode~~electrodes being electrically connected to one of said source region and drain region and extending over ~~said~~the gate ~~electrode~~electrodes;

(b) depositing a dielectric film on said plurality of first ~~electrode~~electrodes;

(c) depositing a conductive film on said dielectric film;

(d) forming a mask layer having a predetermined pattern larger than each of said plurality of first ~~electrode~~electrodes in directions which said data lines and said word lines extend, over said conductive film, and

(e) etching both said conductive film and said dielectric film at a portion exposed from said mask layer in order to form a second ~~electrode~~electrodes for ~~said~~ the plurality of capacitor ~~element~~elements, wherein said ~~etching also etches said dielectric~~

~~film over the other of the source and drain regions of the MISFET~~second electrodes are formed in order to be connected as second electrodes of the capacitor elements of the plurality of memory cells.

2. (Amended) A method of producing a semiconductor integrated circuit device according to claim 1, wherein after said etching, said dielectric film exists only under said second ~~electrode~~electrodes.

4. (Amended) A method of producing a semiconductor integrated circuit device having a plurality of MISFETs arranged in a first direction and in a second direction which is perpendicular to said first direction, each of said plurality of MISFETs having a gate electrode and a source region and a drain region, and a plurality of capacitor elements each having a first electrode respectively connected to one of the source region and the drain region of a respective one of said plurality of MISFETs, a dielectric film and a second electrode, comprising the steps of:

(a) depositing a first conductive film over a semiconductor substrate;

(b) patterning said first conductive film in order to form a plurality of first electrodes for said plurality of capacitor elements, said plurality of first electrodes being arranged in said first and second directions, each of said plurality of first ~~electrode~~electrodes extending respectively over gate electrodes of said plurality of MISFETs;

(c) depositing a dielectric film on said plurality of first ~~electrode~~electrodes;

(d) depositing a second conductive film on said dielectric film; and

(e) etching said second conductive film and said dielectric film in order to form a second ~~electrode~~electrodes for said plurality of capacitor ~~element~~elements and a patterned dielectric film,

wherein said patterned dielectric film has substantially a same pattern as that of the second ~~electrode~~electrodes and exists only under said second ~~electrode~~electrodes, said patterned dielectric film not extending over the other of the source region and the drain region of the respective one of the plurality of MISFETs, and

wherein said second ~~electrode is~~electrodes are larger than said plurality of first ~~electrode~~electrodes in said first and second directions and are formed in order to cover at least each of the one of the source region and the drain region of the plurality of MISFETs.

5. (Amended) A method of producing a semiconductor integrated circuit device having a plurality of MISFETs arranged in a first direction and in a second direction which is perpendicular to said first direction, each of said plurality of MISFETs having a gate electrode and a source region and a drain region, and a plurality of capacitor elements each having a first electrode respectively connected to one of the source region and the drain region of a respective one of said plurality of MISFETs, a dielectric film and a second electrode, comprising the steps of:

(a) forming the plurality of first ~~electrode~~electrodes for the capacitor ~~element~~elements over a semiconductor substrate, each of the plurality of first

~~electrode~~electrodes extending respectively over gate electrodes of said plurality of MISFETs;

(b) depositing a dielectric film on said plurality of first ~~electrode~~electrodes;

(c) depositing a conductive film on said dielectric film; and

(d) patterning said conductive film and said dielectric film respectively to form a second ~~electrode~~electrodes and a patterned dielectric film,

wherein said patterned dielectric film has substantially a same pattern as that of said second ~~electrode~~electrodes, said patterned dielectric film not extending over the other of the source region and the drain region of ~~the respective one~~each of the plurality of MISFETs, and

wherein said second ~~electrode is~~electrodes are larger than said plurality of first ~~electrode~~electrodes in said first and second directions and are formed in order to cover at least each gate electrode of said plurality of MISFETs.

6. (Amended) A method of producing a semiconductor integrated circuit device according to claim 5, wherein said second ~~electrode covers~~electrodes cover both said ~~insulating~~patterned dielectric film and ~~a respective~~the plurality of first ~~electrode~~electrodes.

7. (Amended) A method of producing a semiconductor integrated circuit device according to claim 5, wherein said second ~~electrode covers a respective~~electrodes cover the plurality of first ~~electrode~~electrodes.

Patent ☒ Trademark ☐ 501.26244CC7

Serial No. _____ Filed December 3, 2001

Applicant(s) -MURATA, et al.

Papers filed herewith on December 3, 2001

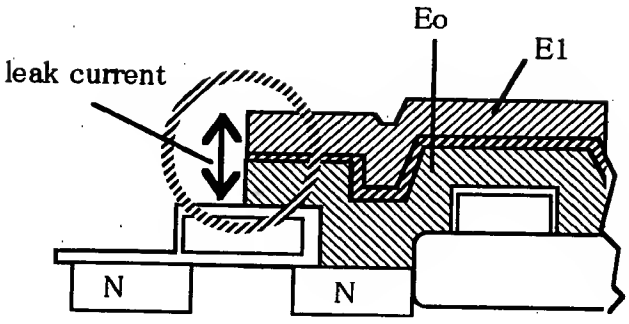
☒ Fees $ 850.00
☐ New Application
☒ Amendment Preliminary
☐ Notice of Appeal
☐ Appeal Brief
☐ Assignment
☐ Letter to Draftsman
☐ Priority Documents
☐ Petition for Ext. of Time
☒ 21 Sheets of Formal Drawings
☒ Other Continuation of application SN 915,590, incld. spec., claims and abstract (118 total pages), copy of decl. information disclosure statement; PTO-1449 Form, claim for priority, terminal disclaimer, utility patent application transmittal, fee transmittal and credit card payment form

Receipt is hereby acknowledged of the papers filed as indicated in connection with above identified case.

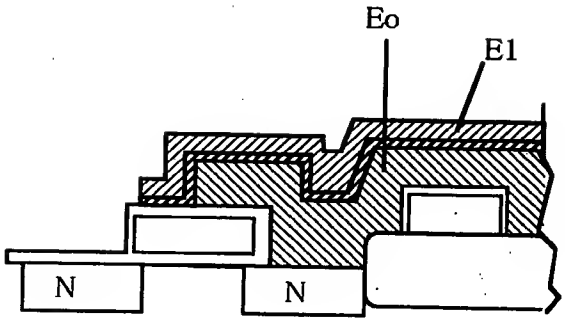
COMMISSIONER OF PATENTS AND TRADEMARKS

APPENDIX

Takemae et al



this invention



DECLARATION

I, Takashi NAKAJIMA, a national of Japan, c/o Central Research Laboratory of Hitachi, Ltd. of 280, Higashi-Koigakubo 1-chome, Kokubunji-shi, Tokyo, Japan, do hereby solemnly and sincerely declare:

1) THAT I am well acquainted with the Japanese language and English language, and
2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No. 62-235913 filed on September 19, 1987.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 9th day of January, 2001.

T. Nakajima

Takashi NAKAJIMA

APPLICATION FOR PATENT

According to the Provision
of Article 38 of Patent Law

September 19, 1987

Hon.

Director-General of Patent Office

Title of the Invention:

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR FABRICATING THE SAME

The number of inventions claimed in the scope of claim for patent: 2

Inventors:

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List of the Annexed Documents:

(1) Specification	one set
(2) Drawings	one set
(3) Power of Attorney	one set
(4) Duplicate of Petition for Patent	one set

Inventors other than the above-mentioned:

Inventors:

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c/o Device Development Center of Hitachi, Ltd.

Hiroko KANEKO

ditto

Shinji SHIMIZU

ditto

SPECIFICATION

1. Title of the Invention

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND PROCESS FOR FABRICATING THE SAME

2. Scope of the Claim

1. A semiconductor integrated circuit device comprising a DRAM constructed of a memory cell composed of a memory cell selecting MISFET and an information storing capacitive element of stacked structure connected in series with one semiconductor region of said MISFET, characterized in that said information storing capacitive element of the stacked structure is constructed of: a first electrode layer connected with the one semiconductor region of said MISFET; a second electrode layer disposed over said first electrode layer to cover the same; and a dielectric film sandwiched between said first electrode layer and said second electrode layer and having substantially the same shape as that of said second electrode layer.

2. A semiconductor integrated circuit device as set forth in Claim 1, characterized in that each of the first and second electrode layers of said information storing capacitive element of the stacked structure is made of a polycrystalline silicon film

into which is introduced an impurity for dropping the resistance.

3. A semiconductor integrated circuit device as set forth in Claim 1 or 2, characterized in that the dielectric film of said information storing capacitive element of the stacked structure is made of a composite film in which are sequentially laminated a silicon oxide film, a silicon nitride film and a silicon oxide film.

4. A semiconductor integrated circuit device as set forth in Claim 3, characterized in that the dielectric film of said information storing capacitive element of the stacked structure is made of a composite film in which are sequentially laminated a natural silicon oxide film, a silicon nitride film deposited by the CVD, and a silicon oxide film formed by oxidizing said silicon nitride film under a high pressure.

5. A process for fabricating a semiconductor integrated circuit device comprising a DRAM constructed of a memory cell composed of a memory cell selecting MISFET and an information storing capacitive element of stacked structure connected in series with one semiconductor region of said MISFET, comprising the steps of: forming said memory cell selecting MISFET;

forming an interlayer insulating film all over the surface of a substrate including that of said MISFET; forming a connection hole, through which is exposed said one semiconductor region, by selectively removing the surface of said interlayer insulating layer over the one semiconductor region of said MISFET; forming a first electrode layer of said information storing capacitive element of the stacked structure in a manner to be connected through said connection hole with said one semiconductor region and to extend over the gate electrode of said MISFET through said interlayer insulating film; forming a dielectric film of said information storing capacitive element all over the surface of said substrate including that of said first electrode layer; and forming a second electrode layer extending over and covering said first electrode layer through said dielectric film, and removing said dielectric film and said interlayer insulating film over the other semiconductor region of said MISFET by using either said second electrode layer or a mask patterning said second electrode layer.

6. A process for fabricating a semiconductor integrated circuit device as set forth in Claim 5, characterized: in that the other semiconductor

region of said MISFET is connected with a data line; and in that the removal of said dielectric film and said interlayer insulating film is accomplished to form a region for said connection.

7. A process for fabricating a semiconductor integrated circuit device as set forth in Claim 5 or 6, characterized in that said interlayer insulating film is used as an etching stopper when each of said first and second electrode layers is patterned.

8. A process for fabricating a semiconductor integrated circuit device as set forth in any of the Claims 5 to 7, characterized in that said first electrode layer has a plane size made larger at least by an extent corresponding to the mask alignment margin of the fabrication step than the opening size of said connection hole to be formed in said interlayer insulating film.

3. Detailed Description of the Invention

[Field of Industrial Application]

The present invention relates to a semiconductor integrated circuit device and, more particularly, to a technique which is effective when applied to a semiconductor integrated circuit device having a DRAM (Dynamic Random Access Memory).

[Prior Art]

The memory cell of the DRAM is composed of a memory cell selecting MISFET and an information storing capacitive element connected in series with one semiconductor region of the MISFET. The memory cell selecting MISFET has its gate electrode connected with a word line extending in a row direction so that it may be controlled by the word line. The other semiconductor region of the memory cell selecting MISFET is connected with a data line extending in a column direction.

The DRAM of this kind has a tendency to be highly integrated for higher capacity and to have its memory cell reduced in size. In case the size of the memory cell is reduced, the size of the information storing capacitive element is also reduced to drop the storage of electric charges for establishing information. This drop of the charge storage is heavily influenced by the minority carriers generated by the alpha rays so that the so-called "soft error" is liable to occur. These phenomena are serious in the DRAM having a large capacity of 1 [Mbit] or more.

Therefore, the information storing capacitive element for the memory cell of the DRAM has adopted the stacked structure (STC). This information storing capacitive element of the stacked structure is

constructed by sequentially laminating a first electrode layer, a dielectric film and a second electrode layer over a semiconductor substrate. The first electrode layer is formed by connecting a portion with one semiconductor region of a memory cell selecting MISFET prepared in advance and by extending the other portion over the gate electrode of the MISFET. Thus first electrode layer thus formed is made of a polycrystalline silicon film which is doped with an impurity (P or As) for reducing the resistance. The dielectric film is made of a silicon oxide film which is prepared by oxidizing the surface of the polycrystalline silicon film of the first electrode layer. The second electrode layer is integrated into a common plate electrode with the second electrode of another adjoining memory cell. The second electrode layer is made of a polycrystalline silicon film like the first electrode layer. With the other semiconductor region of the aforementioned MISFET, there is connected a data line through an intermediate conducting layer which is formed at the fabrication step shared with the aforementioned first electrode layer. Since this intermediate conducting layer is connected in a self-alignment with the other semiconductor region,

the data line is connected in a self-alignment with the other semiconductor region even if the masking displacement is caused at the fabrication steps of the intermediate conducting layer and the data line.

Since the memory cell constructed of the information storing capacitive element of the stacked structure does not use any semiconductor substrate which will generate the minority carriers when it receives the alpha rays, it is advantageous in that it can reduce the soft error. Moreover, the information storing capacitive element of the stacked structure can increase the areas of the first and second electrode layers in the height direction by making use of the stepped shape of the memory cell selecting MISFET. In other words, the information storing capacitive element of the stacked structure can increase the amount of storage of the information establishing electric charges so that its advantage is further reduction of the soft error.

Incidentally, the DRAM having its memory cell constructed of the information storing capacitive element of the stacked structure is disclosed in Japanese Patent Laid-Open No. 61-183952, for example.

[Problems to Be Solved by the Invention]

We have found that the following problems arose

prior to the development of the DRAM of large capacity.

The memory cell of this DRAM is required to have an isolating space between the first electrode layer of the information storing capacitive element of the stacked structure and the aforementioned intermediate conducting layer. That isolating space drops the area of the first electrode layer and accordingly the amount of storage of electric charges of the information storing capacitive element. When, on the other hand, the second electrode layer of the information storing capacitive element of the stacked structure is to be patterned, the intermediate conducting layer uses the dielectric film formed thereover as an etching stopper. Since, however, this dielectric film is made very thin, the intermediate conducting layer is damaged or broken as a result of the overetching on the patterning. This causes poor connection between the other semiconductor region of the MISFET and the data line.

In order to prevent this, it is conceivable not to sandwich the intermediate conducting layer between the other conductive region and the data line. The omission of the intermediate conducting layer can extend the first electrode layer to the

data line to increase the area of the same so that the amount of storage of the electric charges of the information storing capacitive element can be accordingly increased. Since, however, the other semiconductor region has its principal surface substantially exposed to the outside, its principal surface is damaged by the etching when the first and second electrode layers are patterned.

In order to solve this problem, the interlayer insulating film is formed as the etching stopper layer all over the surface of the substrate after the MISFET is formed and before the first electrode layer is formed. The interlayer insulating film used is made of a silicon oxide film which is prepared by the deposition such as CVD. The first electrode layer is formed over the interlayer insulating film, and the connection between the one semiconductor region and the first electrode layer of the MISFET is accomplished through the connection hole which is formed in the aforementioned interlayer insulating film.

Since, however, the interlayer insulating film over the other semiconductor region of the MISFET has to be removed before the data line is connected, there arises a problem that the number of the

fabrication steps increases. Since, moreover, the removal of the interlayer insulating film requires a mask alignment margin at the fabrication steps, there arises another problem that the memory cell area increases to decrease the degree of integration.

On the other hand, let the case be considered in which the dielectric film is used as the etching stopper when the second electrode layer is to be patterned. In this case, the dielectric film left uncovered with the second electrode layer is stored with the electric charges (i.e., charged up) so that its breakdown strength drops. The patterning of the second electrode layer is accomplished by plasma etching, for example. This deteriorates the electric reliability of the DRAM.

An object of the present invention is to provide a technique capable of improving the breakdown strength of the dielectric film of a DRAM which has its memory cell constructed of the information storing capacitive element of stacked structure.

Another object of the present invention is to provide a technique capable of improving the electric reliability of the DRAM while achieving the first-named object.

Still another object of the present invention is

to provide a technique capable of highly integrating the DRAM by reducing the area of the memory cell.

A further object of the present invention is to provide a technique capable of reducing the number of steps of fabricating the DRAM.

The foregoing and other objects and novel features of the present invention will become apparent from the following description to be made with reference to the accompanying drawings.

[Means for Solving the Problems]

The representatives of the invention to be described hereinafter will be summarized in the following.

The information storing capacitive element of the stacked structure of the DRAM has its dielectric film constructed to have the same shape as that of a second electrode layer lying thereover.

Moreover, an interlayer insulating film is removed from the other semiconductor region of a memory cell selecting MISFET by using the second electrode layer or its patterning mask.

[Operations]

According to the means specified above, the dielectric film of the information storing capacitive element of the stacked structure can be coated with

the second electrode layer to reduce the electric charges to be stored in the dielectric film so that the insulating breakdown voltage of the dielectric film can be improved. As a result, it is possible to improve the electric reliability of the DRAM.

Moreover, the interlayer insulating film over the other semiconductor region of the MISFET can be removed by using the second electrode layer or its patterning mask so that the number of steps of fabricating the DRAM can be reduced. Still moreover, the removal of the interlayer insulating film can be accomplished in a self-alignment with respect to the second electrode layer or its patterning mask to that the area of the memory cell can be reduced to improve the degree of integration of the DRAM.

The structure of the present invention will be described in the following in connection with one embodiment thereof, in which the present invention is applied to a DRAM of large capacity.

Incidentally, throughout the drawings for describing the embodiment, the portions having the same functions are designated by common reference characters, and their repeated descriptions will be omitted.

[Embodiment of the Invention]

The DRAM of large memory capacity which is one embodiment of the present invention is shown in Fig. 1 (an equivalent circuit diagram of essential portions).

As shown in Fig. 1, the DRAM is constructed in the folded bit line organization. A memory cell array (memory cell mats) is arranged centrally of Fig. 1.

The memory cell array has complementary data lines DL and $\overline{DL}$ extended in the direction of columns. The complementary data lines DL in a plurality of sets are arranged in the direction of rows. One end side of each set of the complementary data lines DL is connected to a sense amplifier SA.

Word lines WL are extended in the row direction intersecting the complementary data lines DL. The word lines WL in a plurality of number are arranged in the column direction. Each of the word lines WL is laid so as to be connected to and selected by a row decoder circuit X-DEC arranged at an end part of the memory cell array, though this circuit is not shown.

A memory cell M for storing information of 1 [bit] is arranged at the intersection part between each of the complementary data lines DL and the word line WL. The memory cell M is constructed of an n-channel MISFET Q_s for selecting this memory cell, and an information storing capacitor C, one electrode of which is connected in series with one of the semiconductor regions of the MISFET.

The MISFET Q_s of the memory cell M has the other semiconductor region thereof connected to the complementary data line DL, and has the gate electrode thereof connected to the word line WL. The other electrode of the information storing capacitor C is connected to a power source voltage of $\frac{1}{2} V_{CC}$. The power source voltage, $\frac{1}{2} V_{CC}$ is the intermediate potential between the reference voltage V_{SS} (= 0 [V]) of circuitry and the power source voltage V_{CC} (= 5 [V]) of the circuitry. The power source voltage, $\frac{1}{2} V_{CC}$ applied to the other electrode is adapted to lower an electric field intensity which acts across the electrodes of the information storing capacitor C, and to mitigate degradation in the dielectric strength of the dielectric film of the capacitor.

The sense amplifier SA is constructed so as

to amplify the information of the memory cells M which is transmitted by the complementary data lines DL. The information amplified by the sense amplifier SA is delivered to common data lines I/O and $\overline{I/O}$ through Y-switching n-channel MISFETs Q_y.

The Y-switching MISFETs Q_y are so constructed that their gates are connected to and controlled by a Y-select signal line YSL. Each Y-select signal line YSL is laid in correspondence with one set of complementary data lines DL. The Y-select signal lines YSL are extended in the column direction similarly to the complementary data lines DL, and are arranged between the adjacent sets of complementary data lines DL. In other words, the sets of complementary data lines DL and the Y-select signal lines YSL are alternately arranged in the row direction. The Y-select signal lines YSL are constructed so as to be connected to and selected by a column decoder circuit Y-DEC which is arranged at an end part of the memory cell array.

The common data lines I/O are connected to main amplifiers MA which are arranged at an end part of the memory cell array. Each main amplifier MA is connected to an output transistor Dout through switching MISFETs (with no symbols assigned thereto),

output signal lines DOL and $\overline{\text{DOL}}$, and a data output buffer circuit DoB. That is, the information of the memory cells M amplified by the main amplifier MA is delivered to the output transistor Dout through the output signal lines DOL, data output buffer circuit DoB, etc.

Next, there will be described the concrete structures of elements which constitute the memory cells M of the DRAM and the peripheral circuits (sense amplifiers SA, column decoder circuit Y-DEC, etc.) of the DRAM.

The memory cell array of the DRAM is shown in Fig. 2 (a plan view of essential portions), while the elements of the memory cell array and the peripheral circuits are shown in Fig. 3 (a sectional view of essential portions). The left side in Fig. 3 shows the section of the portion of the memory cells M as taken along a cutting-plane line I - I in Fig. 2, and the central part in Fig. 3 shows the section of a guard ring portion as taken along a cutting-plane line II - II in Fig. 2. The right side in Fig. 3 shows the section of complementary MISFETs (CMOS) which constitute the peripheral circuit.

As shown in Figs. 2 and 3, the DRAM is constructed

using a p^--type semiconductor substrate 1 made of single-crystal silicon. A p-type well region 2 is provided in the principal surface parts of the memory cell M (memory cell array)-forming region and n-channel MISFET Q_n-forming region of the semiconductor substrate 1. An n-type well region 3 is provided in the principal surface part of the p-channel MISFET-forming region Q_p of the semiconductor substrate 1. That is, the DRAM of the present embodiment adopts the twin well structure.

An element isolating insulator film (field insulator film) 5 is provided on the principal surface parts of the well regions 2 and 3 between the regions for forming the individual semiconductor elements. The element isolating insulator film 5 is formed so as to electrically isolate the semiconductor elements. A p-type channel stopper region 4A is provided in the principal surface part of the well region 2 under the element isolating insulator film 5. Since a parasitic MOS whose gate insulator film is the element isolating insulator film 5 is liable to inversion into the n-type, the channel stopper region 4A is provided in the principal surface of at least the well region 2.

A p-type potential barrier layer 4B is provided

in the principal surface part of the memory cell M-forming region of the well region 2. The potential barrier layer 4B is provided substantially in the whole surface of the memory cell M-forming region. As will be detailed later, the potential barrier layer 4B is formed by the same manufacturing step and the same manufacturing mask as those of the channel stopper region 4A. The potential barrier layer 4B is constructed in such a way that a p-type impurity (B) introduced into a channel stopper-forming region in order to form the channel stopper region is brought under the memory cell M-forming region by drive-in diffusion.

As shown in Fig. 2, Fig. 3 and Fig. 4 (a plan view of essential portions at predetermined manufacturing steps), the memory cell-selecting MISFETs Q_s of the memory cells M are constructed in the principal surface part of the well region 2 (actually, the potential barrier layer 4B). Each MISFET Q_s has its region surrounded with and its shape defined by the element isolating insulator film 5 and the channel stopper region 4A. Basically, this MISFET Q_s is mainly configured of the well region 2, a gate insulator film 6, a gate electrode 7, and a pair of n-type semiconductor regions 9 which

are a source region and a drain region, respectively.

The well region 2 is used as the channel forming region of the MISFET Q_s.

The gate insulator film 6 is made of a silicon oxide film formed by oxidizing the principal surface of the well region 2.

The gate electrode 7 is provided on the gate insulator film 6, and is made of a polycrystalline silicon film deposited by CVD by way of example. An n-type impurity (P or As) for lowering a resistance is introduced in this polycrystalline silicon film.

Alternatively, the gate electrode 7 may well be formed of the single layer of a refractory metal (Mo, Ti, Ta or W) film or a refractory metal silicide ($MoSi_2$, $TiSi_2$, $TaSi_2$ or WSi_2) film. Further, the gate electrode 7 may well be formed of a composite film in which the above metal film is stacked on a polycrystalline silicon film.

As shown in Figs. 2 and 4, the gate electrodes 7 are constructed to be integral with the word line (WL) 7 which extends in the row direction. That is, the gate electrodes 7 and the word line 7 are formed of the identical conductor layer. The word line 7 is laid so as to connect the gate electrodes 7 of the respective MISFETs Q_s of the plurality of

memory cells M arranged in the row direction.

Regarding the semiconductor regions 9, at least the side (one) to which the information storing capacitor C is connected is formed by ion implantation at an impurity concentration lower than that of the semiconductor regions (17) of a MISFET Q_n constituting the peripheral circuit. Concretely, one of the semiconductor regions 9 is formed by ion implantation at a low impurity concentration below 1×10^{14} [atoms/cm^2]. The inventors' basic research has revealed that, with the semiconductor region 9 formed by the ion implantation at the low impurity concentration below 1×10^{14} [atoms/cm^2], a small number of crystal defects appear in the principal surface part of the well region 2 due to the introduction of an impurity and can be satisfactorily remedied by annealing which is carried out after the introduction of the impurity.

The semiconductor regions 9 are formed in self-alignment to the gate electrode 7. The semiconductor regions 9 construct the MISFET Q_s of the LDD (Lightly Doped Drain) structure because the channel forming region side thereof is made the low impurity concentration.

As shown in Fig. 2, Fig. 3 and Fig. 5 (a plan view of essential portions at predetermined manufacturing

steps), the information storing capacitor C of the memory cell M is mainly configured of a first electrode layer (lower electrode layer) 13, a dielectric film 14 and a second electrode layer (upper electrode layer) 15 which are stacked in succession. The information storing capacitor C is constructed in the so-called stacked structure (STC).

A part (the central part) of the first electrode layer 13 of the information storing capacitor C of the stacked structure is connected to one semiconductor region 9 of the MISFET Q_s. The connection is done through a contact hole 12A which is formed in an inter-layer insulator film 12. The opening size of the contact hole 12A in the column direction is made larger than the length between side-wall spacers 11 which are provided at the respective side walls of the gate electrode 7 of the MISFET Q_s and the word line 7 adjacent thereto. Therefore, the substantial opening size of the contact hole 12A is defined by the length between the side-wall spacers 11. The difference of the opening size of the contact hole 12A and the length between the side-wall spacers 11 is, at least, greater than a component which corresponds to the dimension of a mask registration allowance at a manufacturing

step. Other parts (the peripheral parts) of the first electrode layer 13 are respectively extended on the gate electrode 7 and the word line 7 with the side-wall spacers 11 and inter-layer insulator films 8 interposed therebetween.

The first electrode layer 13 is made of, for example, a polycrystalline silicon film in which an n-type impurity (As or P) for lowering a resistance is introduced at a high concentration. The n-type impurity introduced in the polycrystalline silicon film is diffused to the side of one semiconductor region 9 from the connection part between the first electrode layer 13 and one semiconductor region 9 as defined by the side-wall spacers 11, thereby to form an n^+-type semiconductor region 13A of high impurity concentration which is integral with the semiconductor region 9.

The other part of the first electrode layer 13 is led out in the row direction (upwards or downwards) from a region defined by one set of complementary data lines (21) DL. That is, the first electrode layer 13 is led out of the memory cell M-forming region surrounded with the element isolating insulator film 5. The first electrode layer 13 is spaced so as not to come into contact

with the first electrode layer 13 (formed of the same conductor layer) of the information storing capacitor C of another memory cell M adjacent in the row direction, and the plan shape thereof is made pentagonal in the present embodiment. The first electrode layer 13 is formed so as to extend to a position where this first electrode layer and the Y-select signal line (21) YSL adjacent in the row direction to the complementary data line (21) DL to which the corresponding memory cell M is connected lie one above the other. Since, in actuality, the Y-select signal line (21) YSL overlies the first electrode layer 13, the first electrode layer 13 is formed so as to extend to the position where the Y-select signal line (21) YSL overlaps this first electrode layer.

The dielectric film 14 is basically constructed of a double-layer structure in which a silicon nitride film 14A deposited on the first electrode layer (polycrystalline silicon film) 13 by CVD and a silicon oxide film 14B obtained by oxidizing the silicon nitride film 14A under a high pressure are stacked. Since, in actuality, a natural silicon oxide film is formed on the surface of the polycrystalline silicon film (in which the n-type impurity is introduced)

being the first electrode layer 13, the dielectric film 14 is constructed of a triple-layer structure in which the natural silicon oxide film (not shown, because it has a very small thickness less than 50 [Å]), the silicon nitride film 14A and the silicon oxide film 14B are successively stacked.

Since the silicon nitride film 14A of the dielectric film 14 is deposited by the CVD, it is not affected by the crystal state or stepped shape of the underlying polycrystalline silicon film (first electrode layer 13) and can be formed by process conditions independent of the underlying layer. More specifically, as compared with a silicon oxide film which is formed by oxidizing the surface of the polycrystalline silicon film, the silicon nitride film 14A exhibits a higher dielectric strength and invovles a smaller number of defects per unit area, so that it generates a slight leakage current. Besides, the silicon nitride film 14A has the feature of a higher permittivity over the silicon oxide film. Since the silicon oxide film 14B can be formed into a film of very good quality, the aforementioned characteristics of the silicon nitride film 14A can be further enhanced. In addition, as will be detailed later, the silicon oxide film 14B is

formed by high-pressure oxidation (under 1.5 - 10 [toll]) and can therefore be produced in an oxidation time, namely, annealing time shorter than in normal-pressure oxidation.

The dielectric film 14 is provided along the upper surface and side walls of the first electrode layer 13, and acquires an area in the height direction owing to the utilization of the side wall parts of the first electrode layer 13. The increase of the area of the dielectric film 14 can enlarge the quantity of storage of the charges in the information storing capacitor C of the stacked structure. The dielectric film 14 has its plan shape defined by the shape of the overlying second electrode layer 15, and is formed substantially in the same shape as that of the second electrode layer 15.

The second electrode layer 15 is provided on the dielectric film 14 so as to cover the first electrode layer 13 through this dielectric film. The second electrode layer 15 is made integral with the second electrode layer 15 of the information storing capacitor C of another memory cell M adjoining the corresponding memory cell. The second electrode layer 15 is constructed so as to have the power source voltage of $\frac{1}{2} V_{CC}$ applied thereto. It is

formed of, for example, a polycrystalline silicon film in which an n-type impurity for lowering a resistance is introduced.

The memory cell M thus constructed is connected with another memory cell M adjacent thereto in the column direction. The connection is effected by integrally forming the other semiconductor regions 9 of the respective memory cell-selecting MISFETs Q_s of both the memory cells M.

The complementary data line (DL) 21 is connected to the other semiconductor regions 9 of the MISFETs Q_s of the memory cells M. The complementary data line 21 is connected to the semiconductor regions 9 through a contact hole 19C which is formed in an inter-layer insulator film 19.

As shown in Figs. 2 and 3, an n^+-type semiconductor region 20 of high impurity concentration is provided in the connection part between the complementary data line 21 and the semiconductor regions 9. The semiconductor region 20 is formed in such a way that an n-type impurity (As or P) is introduced through the contact hole 19C by ion implantation. That is, the semiconductor region 20 is formed to be integral with the semiconductor regions 9. When the contact hole 19C undergoes a mask misregistration

at a manufacturing step relative to the semiconductor regions 9 and extends to an end part of the element isolating insulator film 5, the well region 2 and the complementary data line 21 short-circuit. Therefore, the semiconductor region 20 is provided in order to prevent this drawback.

In the present embodiment, the inter-layer insulator film 19 is constructed of a double-layer structure in which a silicon oxide film 19A, and a silicon oxide film (BPSG) 19B capable of glass flow are stacked. The upper silicon oxide film 19B is so constructed that the surface thereof can be flattened by performing the glass flow. The lower silicon oxide film 19A is provided in order to secure a dielectric strength and to prevent B and P, contained in the upper silicon oxide film 19B, from leaking to the element.

The complementary data line 21 is constructed of a triple-layer structure in which a barrier metal film 21A (metal wiring), an aluminum film 21B (metal wiring) and a protective film 21C (metal wiring) are stacked in succession.

The aluminum film 21B is doped with an element for preventing aluminum spikes (Si) and an element for decreasing migration (such as Cu, Pd or Ti).

The aluminum film 21B of the present embodiment is formed by adding about 1.5 [weight-%] of Si and about 0.5 [weight-%] of Cu.

The barrier metal film 21A is constructed so as to prevent single-crystal silicon from precipitating in the connection part between the aluminum film 21A and the semiconductor region 9 (actually, the semiconductor region 20) and the resistance of this connection part from increasing. The barrier metal film 21A is made of $MoSi_2$. Alternatively, the barrier metal film 21A may well be made of a film of any refractory metal silicide other than the above or a film of refractory metal.

The protective film 21C is constructed so as to protect the aluminum film 21B from a liquid which is used in a wet process for forming the aluminum film 21B (for example, a peeling solution process or a water washing process for removing a photoresist film as an etching mask). The aluminum film 21B doped with the element for mitigating the migration (Cu) forms a cell in which aluminum being the base material thereof acts as an anode, while an intermetallic compound produced by the aluminum and Cu acts as a cathode. The cell gives rise to a galvanic reaction with the liquid which

is used in the wet process. The protective film 21C is formed so as to prevent the galvanic reaction. In a case where the galvanic reaction has arisen, the intermetallic compound forms a nucleus, and the surrounding aluminum is scraped off (corrosion takes place).

The protective film 21C is made of $MoSi_x$. Alternatively, the protective film 21C may well be made of a film of any refractory metal silicide ($TiSi_x$, $TaSi_x$ or WSi_x) other than the above or a film of refractory metal. It is formed at a small thickness of about 100 - 4000 [Å].

In the case where the protective film 21C is made of the refractory metal silicide film of $MoSi_x$ or the like, aluminum particles diffuse from the aluminum film 21B, depending upon the content of silicon (Si), so that an aluminum oxide (Al_2O_3) precipitates on the surface of the protective film 21C. The precipitation of the aluminum oxide causes the inferior contact between the protective film 21C and an overlying wiring layer (23). As the result of the inventors' basic research, the content of silicon in $MoSi_x$ for the protective film 21C is set to be greater than 0 and less than 2 ($0 < x < 2$) as illustrated in Figs. 6 thru 8 (diagrams showing

the compositions of wiring as based on the Auger electron spectrometry).

Each of Figs. 6 thru 8 illustrates data obtained in such a way that samples having a structure specified in Fig. 6 (Al-Cu-Si/$MoSi_x$/Si substrate) were annealed at 475 [°C] for 3 hours and thereafter had Al-Cu-Si of the upper layers removed with aqua regia, and that the resulting samples were measured by the Auger electron spectrometry. The axis of abscissas represents the period of time [min.] of sputter etching from the surface of $MoSi_x$. The axis of ordinates represents the intensity of Auger electrons emitted from each of the elements (Mo, Si, O and Al) of the surfaces of the samples in correspondence with various sputtering times. With the Auger electron spectrometry, each time a sample surface is sputter-etched for a predetermined time, the energy of Auger electrons emitted from the sample surface is measured while the sample surface is irradiated with electrons, whereby elements can be identified, and besides, the contents of the elements can be found.

Fig. 6 illustrates the data in the case where the content $\underline{x}$ of silicon was 2, that is, the metal silicide was $MoSi_2$ (MoSi = 1 : 2). As seen from

Fig. 6, in a case where the content x of silicon exceeds 2, aluminum particles having passed through the $MoSi_2$ precipitate at the boundary between the $MoSi_2$ and the Si substrate, and the aluminum particles and oxygen combine to produce the aluminum oxide (Al_2O_3).

Fig. 7 illustrates the data in the case where the content x of silicon was less than 2, that is, the metal silicide was $MoSi_{1.2}$ (Mo : Si = 1 : 1.2), while Fig. 8 illustrates the data in the case where the content x of silicon was 0.8, that is, the metal silicide was $MoSi_{0.8}$ (Mo : Si = 1 : 0.8). As shown in Figs. 7 and 8, in the cases where the content x of silicon is less than 2, the aluminum particles having passed through the $MoSi_x$ do not precipitate at the boundary between the $MoSi_x$ ($x = 0 < x \leq 1.2$) and the Si substrate, and hence, the aluminum oxide is not produced. The inventors' basic research has revealed that the content x of silicon in the protective film 21C should desirably lie in a range greater than 0 and smaller than 1.2.

In the same column direction as the direction in which the complementary data line (DL) 21 extends, the Y-select signal line (YSL) 21 formed of the same conductor layer (the same triple-layer structure)

is extended. As stated before, the first electrode layer 13 of the information storing capacitor C of the stacked structure is led out so as to be positioned under the Y-select signal line 21.

The complementary data lines 21 and the Y-select signal liens 21 (wiring 21) are formed by the step of forming the first layer of wiring in the manufacturing process. The complementary data lines 21 and the Y-select signal lines 21 which are formed by the step of forming the first layer of wiring, are made thinner than the overlying wiring layer (23) in order to moderate a stepped shape peculiar to a multilayer wiring structure.

As shown in Figs. 2 and 3, shunting word lines (WL) 23 are laid on the complementary data lines 21 and Y-select signal lines 21 through an inter-layer insulator film 22 so as to extend in the row direction. Although this is not shown in the drawings, the shunting word line 23 is once led down to an intermediate conductor layer (not shown) through the same contact hole 22D as depicted on the right side (in the peripheral circuit) in Fig. 3 and is connected to the intermediate conductor layer, in every predetermined region which corresponds to several tens - several hundred memory cells M. The intermediate conductor

layers are formed by the step of forming the first layer of wiring, and are connected to the word lines 7 through the contact holes 19C. The shunting word line 23 is constructed so as to lower the resistance of the word line 7. That is, the shunting word line 23 is so constructed that the selection speed of the memory cell M can be raised. The intermediate conductor layer is constructed so as to moderate a stepped shape in the case of connecting the shunting word line 23 and the word line 7, and to prevent the breaking of the shunting word line 23.

As shown in Fig. 3, the inter-layer insulator film 22 is constructed of a triple-layer structure in which a silicon oxide film 22A deposited by plasma CVD, a silicon oxide film 22B formed by coating and subsequent baking, and a silicon oxide film 22C deposited by plasma CVD are stacked in succession. In the inter-layer insulator film 22, the middle silicon oxide film 22B is formed in order to flatten the surface of the upper silicon oxide film 22C.

The contact hole 22D formed in the inter-layer insulator film 22 has a stair shape in vertical section, in which the opening size of an upper side is large, and that of a lower side is small.

The contact hole 22D is provided so as to moderate a stepped shape in the case of connecting the shunting word line 23 and the intermediate conductor layer, and to prevent the breaking of the shunting word line 23.

As shown in Fig. 3, the shunting word line 23 is constructed of a double-layer structure in which an underlying film 23A and an aluminum film 23B are stacked in succession.

The underlying film 23A is made of $MoSi_2$. The $MoSi_2$ can decrease stress migration because Mo enters the aluminum film 23B and can suppress the growth of the crystal grains of the aluminum film 23B. The underlying film 23A may well be made of a film of any refractory metal silicide other than the above or a film of refractory metal.

Likewise to the aluminum film 21B, the aluminum film 23B is doped with Si and Cu.

The shunting word lines 23 are formed by the step of forming the second layer of wiring in the manufacturing process. As compared with the underlying wiring layer (21) formed by the step of forming the first layer of wiring, the shunting word lines 23 which are formed by the step of forming the second layer of wiring are made thicker so as to

lower its resistance.

The upper side in Fig. 2 and the central part in Fig. 3 show an end part of the memory cell array, and a guard ring GL is provided at this part. The guard ring GL is formed so as to enclose the memory cell array, and it is constructed so as to capture minority carriers which are chiefly emitted from a substrate bias generator circuit, not shown. The guard ring GL is formed of a semiconductor region 9 provided in the principal surface part of the well region 2, within a region which is defined by the element isolating insulator film 5 and the channel stopper region 4A. The wiring 21 formed by the step of forming the first layer of wiring is connected to the guard ring GL through the contact hole 19C. The power source voltage of $\frac{1}{2} V_{CC}$ is applied to this wiring 21. In addition, the wiring 21 is connected to the second electrode layer 15 through the contact hole 19C so as to apply the power source voltage of $\frac{1}{2} V_{CC}$ thereto.

In this manner, in a DRAM, one set of complementary data lines (DL) 21 and one Y-select signal line (YSL) 21 for selecting the set of complementary data lines 21 are made of the same conductor layer and are extended in the same column direction,

such complementary data lines 21 and Y-select signal lines 21 are alternately arranged in a row direction, memory cells M each of which is configured of a MISFET Q_s for selecting the memory cell and an information storing capacitor C of stacked structure connected in series with one of the semiconductor regions 9 of the MISFET are connected to the complementary data lines 21, and a first electrode layer 13 constituting the information storing capacitor C of the stacked structure is extended to a position where this electrode layer and the Y-select signal line 21 adjoining the complementary data line 21 to which the corresponding memory cell M is connected lie one above the other, whereby the area of the first electrode layer 13 of the information storing capacitor C of the stacked structure can be increased by utilizing a space where the Y-select signal line 21 is extended, and hence, the quantity of storage of charges in the information storing capacitor C of the stacked structure can be increased. The first electrode layer 13 of the information storing capacitor C of the stacked structure is not formed in a shape symmetric with respect to the complementary data line 21, but is formed in an asymmetric shape led out under the Y-select signal line 21. The

fact that the quantity of storage of charges in the information storing capacitor C of the stacked structure can be increased, makes it possible to diminish soft errors in the memory cell mode of the DRAM. In addition, the fact makes it possible to widen the noise margin of the information readout signals of the DRAM.

CMOS constituting the peripheral circuit are constructed as shown on the right side in Fig. 3. The n-channel MISFET Q_n of the CMOS is formed in the principal surface part of the well region 2, within the region which is surrounded with the element isolating insulator film 5 and the channel stopper region 4A. The MISFET Q_n is mainly configured of the well region 2, a gate insulator film 6, a gate electrode 7, and a pair of n-type semiconductor regions 9 and a pair of n^+-type semiconductor regions 17 which form source and drain regions.

The well region 2, the gate insulator film 6, the gate electrode 7 and the semiconductor regions 9 are respectively formed by the same manufacturing steps of those of the memory cell-selecting MISFET Q_s, and they have similar functions. That is, the MISFET Q_n is constructed in the LDD structure.

The semiconductor regions 17 of high impurity

concentration are constructed so as to lower the respective specific resistances of the source region and the drain region. The semiconductor regions are formed in self-alignment to the gate electrode 7 in such a manner that they are defined by side-wall spacers 11 formed in self-alignment to the side walls of the gate electrode 7.

The wiring 21 to which the reference voltage V_{ss} is applied, is connected through the contact hole 19C to the semiconductor region 17 which is used for the source region. Wiring 21 for an output signal is connected through the contact hole 19C to the semiconductor region 17 which is used for the drain region. A semiconductor region 20 for preventing the short-circuiting between the well region 2 and the wiring 21 is provided in the principal surface part of the well region 2 corresponding to the connection part between the semiconductor region 17 and the wiring 21. These wiring leads are formed by the step of forming the first layer of wiring.

The p-channel MISFET Q_p of the CMOS is formed in the principal surface part of the well region 3, within the region which is surrounded with the element isolating insulator film 5. The MISFET Q_p

is mainly configured of the well region 3, a gate insulator film 6, a gate electrode 7, and a pair of p-type semiconductor regions 10 and a pair of p^+-type semiconductor regions 18 which are a source region and a drain region.

The well region 3, the gate insulator film 6 and the gate electrode 7 have functions substantially similar to those of the corresponding constituents of the MISFET Q_s or Q_n, respectively.

The p-type semiconductor regions 10 of low impurity concentration are provided between the p^+-type semiconductor regions 18 of high impurity concentration and a channel forming region, and they constitute the MISFET Q_p of LDD structure.

The wiring 21 to which the power source voltage V_{cc} is applied, is connected through the contact hole 19C to the semiconductor region 18 which is used for the source region. Wiring 21 for an output signal, which is laid to be integral with the output signal wiring 21 mentioned before, is connected through the contact hole 19C to the semiconductor region 18 which is used for the drain region. These wiring leads 21 are formed by the step of forming the first layer of wiring.

Wiring 23 for an output signal, formed by

the step of forming the second layer of wiring, is connected through the contact hole 22D to the wiring 21 for an output signal.

Next, a concrete method of manufacturing the DRAM will be briefly described with reference to Figs. 9 thru 26 (sectional views of essential portions showing respective predetermined steps of manufacture).

First, a p^--type semiconductor substrate 1 made of single-crystal silicon is prepared. The semiconductor substrate 1 is constructed so as to have a resistivity of, for example, about 8 - 12 [Ω-cm].

Subsequently, a silicon oxide film 24 is formed on the principal surface of the semiconductor substrate 1. The silicon oxide film 24 is formed by steam oxidation at a high temperature of about 900 - 1000 [°C], and to a thickness of, for example, about 400 - 500 [Å].

Subsequently, an oxidation-impermeable film 25 is formed on the silicon oxide film 24. The oxidation-impermeable film 25 is made of, for example, a silicon nitride film deposited by CVD and is formed to a thickness of, for example, about 400 - 600 [Å].

Subsequently, the selected part of the oxidation-

impermeable film 25 corresponding to an n-type well region-forming region is removed, to form an impurity introducing mask and an oxidation-impermeable mask. The selective removal of the oxidation-impermeable film 25 is performed by, for example, photolithography in which etching is carried out with a photoresist film.

Subsequently, as illustrated in Fig. 9, an n-type impurity 3n is introduced selectively into the principal part of the semiconductor substrate 1 through the silicon oxide film 24 in such a way that the oxidation-impermeable film 25 and the photoresist film (not shown) for patterning it are employed as the impurity introducing mask. The n-type impurity 3n used is, for example, P at an impurity concentration on the order of 10^{13} [atoms/cm^2], and is introduced by ion implantation at an energy level of about 120 - 130 [keV].

Subsequently, the photoresist film on the oxidation-impermeable film 25 is removed. Thereafter, as illustrated in Fig. 10, using the oxidation-impermeable film 25 as the oxidation-impermeable mask, the exposed part of the silicon oxide film 24 is grown to form a silicon oxide film 24A. The silicon oxide film 24A is formed on only the n-type

well region-forming region. The silicon oxide film 24A is formed by steam oxidation at a high temperature of about 900 - 1000 [°C] so as to finally become a thickness of, for example, about 1100 - 1200 [Å]. This silicon oxide film 24A is used as an impurity introducing mask in the case of forming a p-type well region. By the oxidation step of forming the silicon oxide film 24A, the introduced n-type impurity 3n is somewhat diffused, so that an n-type semiconductor region (to finally become the well region) 3A is formed.

Subsequently, the oxidation-impermeable film 25 is selectively removed. It is removed with, for example, hot phosphoric acid. Thereafter, as illustrated in Fig. 11, a p-type impurity 2p is introduced selectively into the principal surface part of the semiconductor substrate 1 corresponding to a p-type well region-forming region, through the silicon oxide film 24 by employing the silicon oxide film 24A as the impurity introducing mask. The p-type impurity 2p used is, for example, BF_2 (or B) at an impurity concentration on the order of 10^{12} - 10^{13} [atoms/cm^2], and is introduced by ion implantation. This p-type impurity 2p is not introduced into the principal surface part of the

semiconductor region 3A to become the n-type well region because the silicon oxide film 24A is formed.

Subsequently, as illustrated in Fig. 12, the n-type impurity 3n and the p-type impurity 2p are respectively subjected to drive-in diffusions, to form the n-type well region 3 and the p-type well region 2 as shown in Fig. 12. The well regions 2 and 3 are formed by annealing the substrate in an atmosphere at a high temperature of about 1100 - 1300 [°C]. The p-type well region 2 is consequently formed in self-alignment to the n-type well region 3.

Subsequently, an oxidation-impermeable film 26 is formed on the whole surface of the substrate including both the silicon oxide films 24 and 24A. The oxidation-impermeable film 26 is used as an impurity introducing mask and an oxidation-impermeable mask. The oxidation-impermeable film 26 employed is, for example, a silicon nitride film deposited by CVD and is formed to a thickness of about 400 - 1400 [Å].

Subsequently, the oxidation-impermeable film 26 is coated with a photoresist film, and the part of the photoresist film corresponding to a region for forming an element isolating insulator film (5) is removed, to form an etching mask and an

impurity introducing mask (not shown). Using the mask, the exposed part of the oxidation-impermeable film 26 is selectively removed.

Subsequently, a p-type impurity 4p is introduced into the principal surface of the well region 2 through the exposed silicon oxide film 24 in such a way that a mask which is made up of the oxidation-impermeable film 26 and the photoresist film having patterned it is employed as the impurity introducing mask. The p-type impurity 4p is not introduced into the principal surface part of the well region 3 because the silicon oxide film 24A which is thicker as compared with the silicon oxide film 24 is formed on the principal surface of the well region 3. That is, the p-type impurity 4p is introduced selectively into the principal surface of the well region 2. It is adapted to form a channel stopper region and a potential barrier layer. It is introduced by ion implantation by employing BF_2 or B at an impurity concentration on the order of 10^{13} [atoms/cm^2]. After the p-type impurity 4p has been introduced, the photoresist film on the oxidation-impermeable film 26 is removed as shown in Fig. 13.

Subsequently, using the oxidation-impermeable film 26 as the oxidation-impermeable mask, the

exposed parts of both the silicon oxide films 24 and 24A are grown to form the element isolating insulator film (field insulator film) 5. The element isolating insulator film 5 is formed, for example, in such a way that annealing for about 110 - 130 [min.] is carried out in a nitrogen gas atmosphere at a high temperature of about 1000 [°C], whereupon steam oxidation is carried out for about 150 - 160 [min.]. Alternatively, it is formed by the use of only a steam oxidation atmosphere. The element isolating insulator film 5 is formed to a thickness of, for example, about 6000 - 8000 [Å].

By substantially the same manufacturing step as the step of forming the element isolating insulator film 5, the p-type impurity 4p introduced in the principal surface part of the well region 2 undergoes the drive-in diffusion, and the p-type channel stopper region 4A is formed. In forming this channel stopper region 4A, the annealing which is comparatively long as stated above is carried out, so that the lateral diffusion is extensive as illustrated in Fig. 27 (an impurity concentration profile). Especially in a memory cell array, the p-type impurity 4p is diffused into nearly the whole surface of a region for forming memory cells M, and the p-type

potential barrier layer 4B is formed.

In Fig. 27, the axis of abscissas represents the depth [μm] of the well region 2 from the surface thereof, and the axis of ordinates the concentration of the p-type impurity (boron) 4p. As seen from Fig. 27, when the distribution of the p-type impurity 4p at the introduction thereof (a dotted line) is compared with the distribution thereof after the execution of the above-stated annealing (a solid line), the impurity diffuses about 0.4 - 0.6 [μm]. In a DRAM of large memory capacity, the dimension of the gate width (channel width) of the memory selecting MISFET Q_s of the memory cell M and the dimension of the semiconductor region 9 of the MISFET in the direction of the gate width are about 1.0 [μm]. Therefore, the p-type impurity 4p forming the channel stopper region 4A diffuses into nearly the whole surface of the memory cell M-forming region, and the potential barrier layer 4B is formed in nearly the whole surface of the memory cell M-forming region as stated before.

In a region for forming an n-channel MISFET Q_n which constitutes the CMOS of a peripheral circuit, the p-type impurity 4p is diffused into only a part of the vicinity of the element isolating insulator

film 5, and in effect, the potential barrier layer 4B is not formed, because the size of the MISFET Q_n is larger than that of the memory cell M. That is, the potential barrier layer 4B is not formed in the region for forming the MISFET Q_n of the peripheral circuit, and it is formed selectively in the memory cell array-forming region. Moreover, it can be formed by the same manufacturing step as that of the channel stopper region 4A.

Both the channel stopper region 4A and the potential barrier layer 4B are constructed at an impurity concentration on the order of 10^{16} - 10^{17} [atoms/cm^3] after the annealing. After the channel stopper region 4A and the potential barrier layer 4B have been formed, the oxidation-impermeable film 26 is selectively removed as illustrated in Fig. 14.

In this manner, in a DRAM wherein each memory cell M is surrounded with an element isolating insulator film 5 and a channel stopper region 4A, a p-type impurity 4p which has the same conductivity type as that of a well region 2 and which is at a concentration higher than that of the well region 2 is introduced into the principal surface part of the well region 2 among the MISFETs Q_s of the

memory cells M, and in the principal surface part of the well region 2, the p-type impurity 4p is diffused to, at least, under a region for forming one semiconductor region (a side to be connected with an information storing capacitor C) 9 of the MISFET Q_s, to form the channel stopper region 4A and a potential barrier layer 4B, and to form the element isolating insulator film 5 on the principal surface of the well region 2 among the MISFETs, whereby the step of forming the channel stopper region 4A serves also as the step of forming the potential barrier layer 4B, and hence, the number of the manufacturing steps of the DRAM can be decreased. That is, a mask forming step and an impurity introducing step for forming the potential barrier layer 4B can be dispensed with.

In addition, since the potential barrier layer 4B can be formed in self-alignment to both the element isolating insulator film 5 and the channel stopper region 4A, the dimension of a mask registration allowance in the manufacturing process can be dispensed with. The exclusion of the dimension of the mask registration allowance makes it possible to reduce the area of the memory cell M of the DRAM, and therefore to heighten the density of integration.

Besides, since the p-type impurity 4p introduced for forming the channel stopper region 4A is sufficiently diffused in the potential barrier layer 4B by annealing, the damages of the well region 2 attributed to the impurity introduction can be remedied to decrease crystal defects. The decrease of the crystal defects can enhance the refresh characteristics of the DRAM.

By the way, in a case where the potential barrier layer 4B is formed in the whole surface of a memory cell M-forming region, a memory cell array need not be provided with the well region 2.

After the step of removing the oxidation-impermeable film 26 as illustrated in Fig. 14, the silicon oxide film 24 on the principal surface of the well region 2 and the silicon oxide film 24A on the principal surface of the well region 3 are removed to expose the principal surfaces of the respective well regions 2 and 3.

Subsequently, a silicon oxide film 6A is formed on the exposed principal surfaces of both the well regions 2 and 3. The silicon oxide film 6A is formed for the purpose of oxidizing so-called white ribbons being a nitride film of silicon which is formed at the end parts of the element isolating

insulator film 5 by the oxidation-impermeable film (silicon nitride film) 26 in forming the element isolating insulator film 5. The silicon oxide film 6A is formed by steam oxidation at a high temperature of about 900 - 1000 [°C], and to a thickness of about 400 - 1000 [Å].

Subsequently, a p-type impurity 27p for adjusting the threshold voltage of each n-channel MISFET is introduced into the principal surface parts of both the well regions 2 (the potential barrier layer 4B in the memory cell array) and 3, namely, the whole surface of the substrate, within an element forming region which is defined by the element isolating insulator film 5. The p-type impurity 27p used is B at an impurity concentration on the order of 10^{11} [atoms/cm^2], and is introduced by ion implantation at an energy level of about 30 [keV].

Subsequently, as illustrated in Fig. 15, a p-type impurity 28p for adjusting the threshold voltage of each p-channel MISFET is introduced selectively into the principal surface of the well region 3 within the element forming region which is defined by the element isolating insulator film 5. The p-type impurity 28p used is B at an impurity

concentration on the order of 10^{12} [atoms/cm^2], and is introduced by ion implantation at an energy level of about 30 [keV]. These steps of introducing the respective p-type impurities 27p and 28p for adjusting the threshold voltages can be omitted in some ways of setting the impurity concentrations of the respective well regions 2 and 3.

Subsequently, the silicon oxide film 6A is selectively removed to expose the principal surfaces of both the well regions 2 and 3. It is removed by wet etching.

Subsequently, a gate insulator film 6 is formed on the exposed principal surfaces of both the well regions 2 and 3. The gate insulator film 6 is formed by steam oxidation at a high temperature of about 800 - 1000 [°C], and to a thickness of about 150 - 250 [Å].

Subsequently, a polycrystalline silicon film is formed on the whole surface of the substrate including the gate insulator film 6 and the element isolating insulator film 5. The polycrystalline silicon film is deposited by CVD, and is formed to a thickness of about 2000 - 3000 [Å]. This polycrystalline silicon film is formed by the step of forming the first layer of gate wiring in the

manufacturing process. Thereafter, P is introduced into the polycrystalline silicon film by thermal diffusion so as to lower the resistance of this polycrystalline silicon film.

Subsequently, an inter-layer insulator film 8 is formed on the whole surface of the polycrystalline silicon film. The inter-layer insulator film 8 is chiefly intended to electrically isolate the polycrystalline silicon film and a conductor layer overlying it. The inter-layer insulator film 8 used is, for example, a silicon oxide film deposited by CVD, and it is formed to a thickness of about 3500 - 4500 [Å].

Subsequently, as illustrated in Fig. 16, the inter-layer insulator film 8 and the polycrystalline silicon film are successively etched to form gate insulator films 7 and word lines (WL) 7, by employing an etching mask formed of a photoresist film not shown. Since the inter-layer insulator film 8 and the polycrystalline silicon film are stackedly etched, parts of the inter-layer insulator film 8 in the same shapes are left on both gate electrodes 7 and the word lines 7. The step of forming the first layer of gate wiring forms the gate electrodes 7 of the MISFETs Q_s and the word lines 7 in the

memory cell array, and also forms the gate electrodes 7 of the MISFETs Q_n and Q_s of the peripheral circuits. Besides, the step of forming the first layer of gate wiring is adapted to form resistors and wiring leads for connecting elements though they are not shown. As the above etching, anisotropic etching such as RIE is employed. Thereafter, the photoresist film is removed.

Subsequently, in order to mitigate contamination ascribable to the impurity introduction, a silicon oxide film (not shown) is formed on the exposed principal surfaces of both the well regions 2 and 3 (including the side walls of the gate electrodes 7 and the word lines 7). By way of example, the silicon oxide film is formed in an oxygen gas atmosphere at a high temperature of about 850 - 950 [°C], and to a thickness of about 100 - 800 [Å].

Subsequently, using the element isolating insulator film 5 and the inter-layer insulator film 8 as an impurity introducing mask, an n-type impurity is introduced selectively into the principal surface parts of the well region 2 corresponding to the memory cell array-forming region and the n-channel MISFET Q_n-forming region. By the introduction of the n-type impurity, n-type semiconductor regions

9 of low impurity concentration are formed in self-alignment to the respective gate electrodes 7 and word lines 7. As the n-type impurity for forming the semiconductor regions 9, P (or As) at an impurity concentration on the order of 10^{13} [atoms/cm^2] is employed, and it is introduced by ion implantation at an energy level of about 60 - 120 [keV]. As described before, at least that semiconductor region 9 of the memory cell-selecting MISFET Q_s of the memory cell M which is connected to the information storing capacitor C is formed by ion implantation at a low impurity concentration less than 10^{14} [atoms/cm^2]. Since the semiconductor region 9 is formed at the low impurity concentration, each of the MISFETs Q_s and Q_n can be constructed in the LDD structure. In forming the semiconductor regions 9, the p-channel MISFET Q_p-forming region is covered with an impurity introducing mask which is formed of a photoresist film. In addition, as will be described later, the MISFET Q_n constituting the CMOS of the peripheral circuit has its source region and drain region constructed of the semiconductor regions 9, and semiconductor regions 17 which are formed by ion implantation at a high impurity concentration of or above 10^{14} [atoms/cm^2]. The memory cell-

selecting MISFETs Q_s of the memory cells M are substantially finished up by the step of forming the semiconductor regions 9.

In this manner, in a DRAM wherein each memory cell M includes an information storing capacitor C of stacked structure, one of the semiconductor regions 9 of the MISFET Q_s of the memory cell M is constructed by ion implantation at an impurity concentration lower than that of the high impurity concentration-semiconductor regions 17 of each of the MISFETs Q_n of peripheral circuits other than the memory cells M, whereby the apperance of crystal defects in the surface of a well region 2 attributed to the ion implantation for forming a source region or a drain region can be mitigated, and the leakage of charges stored in the information storing capacitor C and to serve as information can be lessened, so that the refresh characteristics of the DRAM can be enhanced. The enhancement of the refresh characteristics can raise the speeds of the information writing operation and information reading operation of the DRAM.

Besides, since the MISFET Q_s of the memory cell M has the channel forming region side thereof constructed of the semiconductor region 9 of low

impurity concentration, the short-channel effect can be suppressed, and the area of the memory cell M can be reduced. That is, the semiconductor region 9 can raise the density of integration of the DRAM.

Moreover, the semiconductor regions 9 of the MISFET Q_s of the memory cell M are formed by the same manufacturing step as that of semiconductor regions 9 for constructing the LDD structure of the MISFET Q_n of the CMOS of the peripheral circuit, whereby the step of the ion implantation of low impurity concentration for the MISFET Q_s is not separately added, but it is simultaneously performed by the step of forming the semiconductor regions 9 of the MISFET Q_n, so that the number of the manufacturing steps of the DRAM can be decreased.

Besides, especially in a memory cell M-forming region, a potential barrier layer 4B is formed by the diffusion of the p-type impurity 4p of a channel stopper region 4A, and the impurity concentrations of the two can be set within a low range on the order of 10^{16} - 10^{17} [atoms/cm^3], so that the breakdown voltage of the p-n junction between the semiconductor region 9 of the MISFET Q_s and the potential barrier layer 4B or channel stopper region 4A can be enhanced. That is, in a DRAM wherein each memory cell M is

surrounded with an element isolating insulator film 5 and a channel stopper region 4A, a potential barrier layer 4B formed by diffusing the p-type impurity 4p of the channel stopper region 4A is provided in the principal surface part of a well region 2 under at least one semiconductor region (on a side connected to an information storing capacitor C) 9 of the MISFET Q_s of the memory cell M, whereby the capture of minority carriers into the information storing capacitor C can be relieved by the potential barrier layer 4B, so that the soft errors of a memory cell mode can be prevented, and besides, the impurity concentration of the channel stopper region 4A and that of the potential barrier layer 4B can be made substantially the same impurity concentration, to enhance the breakdown voltage of the p-n junction between the channel stopper region 4A or potential barrier layer 4B and one semiconductor region 9 mentioned above, so that the leakage of the charges of the information storing capacitor C to serve as information can be lessened to enhance information retention characteristics. The enhancement of the information retention characteristics can enhance the refresh characteristics of the DRAM, and can heighten the speeds of the information

writing operation and information reading operation thereof.

Further, in the DRAM stated above, the potential barrier layer 4B is provided in the principal surface parts of the well region 2 under one semiconductor region 9 and the other semiconductor region (on a side connected to a complementary data line 21) 9 of the MISFET Q_s of the memory cell M, whereby in addition to the aforementioned effects, the soft errors of a data line mode can be prevented, so that the information retention characteristics can be more enhanced.

Subsequently, after the step of forming the semiconductor regions 9, using the element isolating insulator film 5 and the inter-layer insulator film 8 as an impurity introducing mask, a p-type impurity is introduced selectively into the principal surface part of the well region 3 corresponding to a p-channel MISFET Q_p-forming region. As shown in Fig. 17, p-type semiconductor regions 10 of low impurity concentration self-aligned to the gate electrode 7 are formed by the introduction of the p-type impurity. As the p-type impurity for forming the semiconductor regions 10, BF_2 (or B) at an impurity concentration on the order of

10^{13} [atoms/cm^2] is employed, and it is introduced by ion implantation at an energy level of about 60 - 100 [keV]. In forming the semiconductor regions 10, the memory cell array-forming region and the n-channel MISFET Q_n-forming region are covered with impurity introducing masks which are formed of photoresist films.

Subsequently, although not illustrated in the drawings, an n-type impurity is introduced at a high impurity concentration into, at least, a region for forming the drain region of an n-channel MISFET (an electrostatic breakdown preventing circuit) which constitutes the input/output circuit of the DRAM. Owing to the additional introduction of the n-type impurity, this MISFET constituting the input/output circuit can render an excess voltage easy of leaking to the side of the well region 2, the excess voltage entering the drain region and giving rise to electrostatic breakdown, and can enhance an electrostatic breakdown voltage.

Subsequently, as illustrated in Fig. 18, side-wall spacers 11 are formed on the side walls of each of the gate electrodes 7 and the word lines 7. The side-wall spacers 11 can be formed in such a way that a silicon oxide film deposited by CVD

is subjected to anisotropic etching such as RIE. The silicon oxide film is formed at a thickness of, for example, about 3500 - 4500 [Å]. The length of the side-wall spacer 11 in the gate length direction (channel length direction) thereof is made about 2500 - 4000 [Å]. On this occasion, if necessary, the side-wall spacers may well be formed by etching after their regions have been limited with a photoresist film.

Subsequently, an inter-layer insulator film 12 is formed on the whole surface of the substrate including the inter-layer insulator film 8, the side-wall spacers 11, etc. The inter-layer insulator film 12 is used as an etching stopper in the case of patterning each of a first electrode layer (13) and a second electrode layer (15) which constitute the information storing capacitor C of stacked structure. For this reason, the inter-layer insulator film 12 is formed at a thickness at which the amounts of scrape ascribable to overetching in the operations of etching the first electrode layer and the second electrode layer, the amounts of scrape at washing steps to be carried out before the formation of the second electrode layer, and so on. The inter-layer insulator film 12 is formed so that, especially

in patterning the first electrode layer and the second electrode layer, damages attributed to the etching operations may be prevented from arising in the surface of the other semiconductor region (to which the complementary data line 21 is connected) 9 of the memory cell-selecting MISFET Q_s. By way of example, the inter-layer insulator film 12 is made of a silicon oxide film deposited at a high temperature of about 700 - 800 [°C] and by CVD, and it is formed at a thickness of about 1000 - 2000 [Å].

Subsequently, as illustrated in Fig. 19, the part of the inter-layer insulator film 12 on one semiconductor region (to which the first electrode layer 13 of the information storing capacitor C is connected) 9 of each of the MISFETs Q_s in the memory cell M-forming region is selectively removed to form a contact hole 12A. In the direction of columns, the contact hole 12A is formed into a size which is larger, at least, a component corresponding to the dimension of a mask registration allowance in the manufacturing process, as compared with a size that is defined by the side-wall spacer 11 on the side wall of the gate electrode 7 of the MISFET Q_s and the side-wall spacer 11 on the

side wall of the word line 7 adjoining this gate electrode. That is, as regards the contact hole 12A, the substantial size thereof in which the semiconductor region 9 is exposed is defined by the side-wall spacers 11.

Subsequently, as illustrated in Fig. 20, there are formed the first electrode layers 13 each of which has a part connected to the semiconductor region 9 through the contact hole 12A and has other parts extended on the gate electrode 7 and the word line 7 through the inter-layer insulator films 8 and 12. The first electrode layer 13 constructs the lower electrode layer of the information storing capacitor C of the stakced structure. This first electrode layer 13 is formed to be larger, at least, a component corresponding to the dimension of a mask registration allowance in the manufacturing process, as compared with the size of the contact hole 12A formed in the inter-layer insulator film 12. In a case where the size of the first electrode layer 13 is not larger than that of the contact hole 12A by the above value, an end part of the first electrode layer 13 falls into the contact hole 12A, and an unnecessary groove appears between the peripheral wall of the contact hole 12A and

the side wall of the end part of the first electrode layer 13. When a photoresist film for patterning the first electrode layer 13 is applied, it is formed to be thicker in the part of the groove than in the other area, and halation occurs in the developing operation of the photoresist film, resulting in the inferior shape of the first electrode layer 13.

The first electrode layer 13 is formed of polycrystalline silicon deposited by CVD, and to a thickness of about 800 - 3000 [Å]. The polycrystalline silicon film is formed in such a way that a silicon oxide film is first formed on the surface, that an n-type impurity for lowering a resistance is introduced through the silicon oxide film, and that the silicon oxide film is removed after annealing. The silicon oxide film is formed by oxidizing the surface of the polycrystalline silicon film with steam, and to a thickness of about 100 [Å]. The n-type impurity used is As or P at an impurity concentration on the order of 10^{15} [atoms/cm^2], and is introduced by ion implantation at an energy level of about 75 - 85 [keV]. The patterning of the polycrystalline silicon film is performed by dry etching. In etching the polycrystalline silicon

film, the inter-layer insulator film 12 is used as the etching stopper layer. This first electrode layer 13 is formed by the step of forming the second layer of gate wiring.

The n-type impurity introduced into the first electrode layer (polycrystalline silicon film) 13 by the annealing after the n-type impurity introduction, is diffused into that principal surface part of the well region 2 (actually, the semcionductor region 9) in which the first electrode layer 13 and one semiconductor region 9 are connected. An n^+-type semiconductor region 13A of high impurity concentration is formed by the diffusion. The semiconductor region 13A is constructed to be integral with the semiconductor region 9. While the semiconductor region 13A constitutes one semiconductor region of the memory cell-selecting MISFET Q_s, it is chiefly intended to enhance the ohmic contact between the semiconductor region 9 and the first electrode layer 13 (lowering the contact resistance).

Incidentally, the first electrode layer 13 inside the contact hole 12A is electrically isolated from each of the gate electrode 7 and the word line 7 through the inter-layer insulator film 8 and the side-wall spacer 11.

Subsequently, as illustrated in Fig. 21, a dielectric film 14 is formed on the whole surface of the substrate including the first electrode layer 13. As stated before, the dielectric film 14 is basically formed of a double-layer structure in which a silicon nitride film 14A and a silicon oxide film 14B are successively stacked.

The silicon nitride film 14A is deposited on the first electrode layer (polycrystalline silicon film) 13 by CVD, and is formed at a thickness of about 50 - 100 [Å]. In forming this silicon nitride film 14A, the involvement of oxygen is suppressed to the utmost. In a case where the silicon nitride film 14A is formed on the polycrystalline silicon film at an ordinary production level, a very slight amount of oxygen is involved, and hence, a natural silicon oxide film (not shown) is formed between the first electrode layer 13 and the silicon nitride film 14A. Accordingly, the dielectric film 14 is constructed of a triple-layer structure in which the natural silicon oxide film, the silicon nitride film 14A and the silicon oxide film 14B are successively stacked. The natural silicon oxide film can be thinned when the involvement of oxygen is diminished. Alternatively, the dielectric film 14 can be constructed

of a double-layer structure by nitrifying the natural silicon oxide film though this measure adds to the manufacturing step.

The silicon oxide film 14B is formed to a thickness of about 10 - 60 [Å] by oxidizing the silicon nitride film 14A of the lower layer under a high pressure. When the silicon oxide film 14B is formed, the silicon nitride film 14A is somewhat decreased, and hence, it is finally formed to a thickness of about 40 - 80 [Å]. Basically, the silicon oxide film 14B is formed in an oxygen gas atmosphere having a high pressure of 1.5 - 10 [toll] and a high temperature of about 800 - 1000 [°C]. In the present embodiment, the silicon oxide film 14B is formed under a high pressure of 3 - 3.8 [toll] and by setting the flow rate of oxygen (a source gas) at 2 [l./min.] and the flow rate of hydrogen (a source gas) at 3 - 8 [l./min.] during the oxidization. As illustrated in Fig. 28 (a diagram showing the oxidization characteristics of silicon nitride films), the silicon oxide film 14B which is formed by the high-pressure oxidization can be formed to a desired thickness in a shorter period of time as compared with a silicon oxide film which is formed under the normal pressure

(1 [toll]). In Fig. 28, the oxidizing period of time [min.] is indicated on the axis of abscissas, and the thickness [Å] of an oxide film on a silicon nitride film (Si_3N_4) is indicated on the axis of ordinates. That is, the high-pressure oxidization shortens the period of time of annealing at a high temperature and can form a dielectric film of good quality. Since the shortening of the oxidizing period of time can decrease the p-n junction depths of the source regions and drain regions of the MISFETs Q_s, Q_n and Q_p, the microfabrication of the MISFETs can be achieved.

In this manner, in a DRAM having an information storing capacitor C of stacked structure, the first electrode layer 13 of the information storing capacitor C is made of a polycrystalline silicon film in which an impurity for lowering a resistance is introduced, and a dielectric film 14 is configured of a silicon nitride film 14A deposited on the first electrode layer 13 and a silicon oxide film 14B formed on the silicon nitride film 14A by subjecting the surface thereof to high-pressure oxidization, whereby the silicon nitride film 14A of uniform thickness can be formed without being affected by the crystal state and shape of the surface of

the underlying first electrode layer 13, and the silicon oxide film 14B of good quality can be formed on this silicon nitride film 14A, so that enhancement in the dielectric strength of the dielectric film 14, decrease in the number of the defects of the dielectric film 14 per unit area and decrease in the leakage current of the dielectric film 14 can be achieved, and a period of time for forming the silicon oxide film 14B can be shortened, so that elements can be microfabricated to raise the density of integration.

Alternatively, the dielectric film 14 of the information storing capacitor C of the stacked structure may well be constructed of a quadruple-layer structure in which the natural silicon oxide film, the silicon nitride film 14A, the silicon oxide film 14B and a silicon nitride film are successively stacked. With the dielectric film 14 of the triple-layer structure described before, current flows more in a case where the electrode layer (15) of the upper side is a negative electrode, than in a case where it is a positive electrode, so that the initial dielectric strength of the dielectric film is low. The dielectric film 14 of the quadruple-layer structure is provided with the silicon nitride

film between the silicon oxide film 14B and the electrode layer (15) of the upper layer, and can enhance the initial dielectric strength thereof.

Subsequently, a polycrystalline silicon film for constructing the second electrode layer (15) is formed on the whole surface of the dielectric film 14. The polycrystalline silicon film is deposited by CVD, and is formed at a thickness of about 1500 - 2500 [Å]. This polycrystalline silicon film is formed by the step of forming the third layer of gate wiring in the manufacturing process.

Subsequently, an n-type impurity for lowering a resistance is introduced into the polycrystalline silicon film. Phosphorus is used as the n-type impurity, and is introduced into the polycrystalline silicon film by thermal diffusion. The n-type impurity is introduced so that the sheet resistance of the polycrystalline silicon film may become 20 - 100 [Ω/□].

Subsequently, the whole surface of the polycrystalline silicon film is coated with a photoresist film. Thereafter, the parts of the photoresist film on regions for forming the second electrode layers (15) of the information storing capacitors C of the memory cells M are photolithographically left

unetched, to form an etching mask 29 (indicated by dotted lines).

Subsequently, using the etching mask 29, the polycrystalline silicon film is etched to form the second electrode layers 15. As the etching, plasma etching is used. Thereafter, as illustrated in Fig. 22, the exposed parts of the dielectric film 14 and the underlying inter-layer insulator film 12 are successively etched by employing the etching mask 29 (which may well be replaced with the second electrode layers 15) again. As this etching, dry etching is used. The dielectric film 14 is formed substantially in the same shape as that of the second electrode layer 15 so as to exist only under this electrode layer. The parts of the dielectric film 14 and the inter-layer insulator film 12 on the other regions (to which the complementary data lines 21 are connected) 9 of the MISFETs Q_s of the memory cells M and on the regions for forming both the MISFETs Q_n and Q_p of the peripheral circuits, are removed by the etching.

By the step of forming the second electrode layers 15, the information storing capacitors C of the stacked structure constituting the memory cells M are nearly finished up. Simultaneously,

the memory cells M are nearly finished up.

In this manner, in a DRAM wherein each memory cell M includes an information storing capacitor C of stacked structure, the information storing capacitor C of the stacked structure is configured of a first electrode layer 13 which is connected to one semiconductor region 9 of a MISFET Q_s, a second electrode layer 15 which is provided over the first electrode layer 13 so as to cover it, and a dielectric film 14 which is interposed between the first electrode layer 13 and the second electrode layer 15 and which has substantially the same shape as that of the second electrode layer 15, whereby the dielectric film 14 is covered with the second electrode layer 15, and the accumulation of charges in the dielectric film 14 (the charge-up of the dielectric film 14) at the step of patterning the second electrode layer 15 or at a later step can be relieved, so that the degradation of the dielectric strength (characteristics) of the dielectric film 14 attributed to the accumulation of the charges can be prevented. The prevention of the degradation of the dielectric strength of the dielectric film 14 can enhance the electrical reliability of the DRAM.

Besides, in a DRAM wherein each memory cell M includes an information storing capacitor C of stacked structure, a MISFET Q_s for selecting the memory cell is formed, an inter-layer insulator film 12 which covers the MISFET Q_s is formed, the part of the inter-layer insulator film 12 on one semiconductor region 9 of the MISFET Q_s is selectively removed to form a contact hole 12A through which the aforementioned semiconductor region 9 is exposed, that first electrode layer 13 of the information storing capacitor C of the stacked structure which is connected to the aforementioned semiconductor region 9 through the contact hole 12 and which is extended over the gate electrode 7 of the MISFET Q_s through the insulator film 12 is formed, a dielectric film 14 is formed on the first electrode layer 13, a second electrode layer 15 which overlies the first electrode layer 13 through the dielectric film 14 is formed, and using the second electrode layer 15 or a mask 29 for patterning it, at least the part of the inter-layer insulator film 12 on the other semiconductor region 9 of the MISFET Q_s is removed, whereby the second electrode layer 12 or the mask 29 can be used aslo as a mask for removing the part of the inter-layer insulator

film 12 on the other semiconductor region 9 on a side which is connected with the complementary data line (21) of the MISFET, so that the step of forming the mask for removing the inter-layer insulator film 12 can be omitted.

Moreover, the part of the inter-layer insulator film 12 on the other semiconductor region 9 of the MISFET Q_s can be removed in self-alignment to the second electrode layer 12 because of the use of the same mask, so that the area of the memory cell M can be reduced in correspondence with the dimension of a mask registration allowance in a manufacturing process. As a result, the density of integration of the DRAM can be heightened.

Subsequently, an insulator film 16 is formed on the whole surface of the substrate. The insulator film 16 is formed on the semiconductor regions 9 and 10 being source and drain regions, at least within the region for forming the CMOS of the peripheral circuits. By way of example, the insulator film 16 is formed of a silicon oxide film deposited by CVD and to a thickness of about 300 [Å].

Subsequently, an n-type impurity is introduced selectively into the principal surface of the well region 2 within each region for forming the n-channel

MISFET Q_n which constitutes the CMOS of the peripheral circuit. The introduction of the n-type impurity is carried out by mainly employing the gate electrode 7 and the inter-layer insulator film 8 as an impurity introducing mask, in the state in which the memory cell M-forming region and the p-channel MISFET Q_p-forming region are covered with a photoresist film. The n-type impurity used is, for example, As at an impurity concentration on the order of 10^{15} [atoms/cm^2], and is introduced by ion implantation at an energy level of about 70 - 90 [keV].

Subsequently, a p-type impurity is introduced selectively into the principal surface part of the well region 3 within each region for forming the p-channel MISFET Q_p which constitutes the CMOS of the peripheral circuit. The introduction of the p-type impurity is carried out by mainly employing the gate electrode 7 and the inter-layer insulator film 8 as an impurity introducing mask, in the state in which the memory cell M-forming region and the n-channel MISFET Q_n-forming region are covered with a photoresist film. The p-type impurity used is, for example, BF_2 at an impurity concentration on the order of 10^{15} [atoms/cm^2], and is introduced by ion implantation at an energy level of about

70 - 90 [keV].

Thereafter, the n-type impurity and the p-type impurity are subjected to drive-in diffusions, to form n^+-type semiconductor regions 17 in the principal surface parts of the well region 2 and p^+-type semiconductor regions 18 in the principal surface parts of the well region 3 as shown in Fig. 23. The drive-in diffusions are carried out at a high temperature of about 900 - 1000 [°C] for about 10 [min.]. The MISFET Q_n is nearly finished up by the step of forming the semiconductor regions 17, while the MISFET Q_p is nearly finished up by the step of forming the semiconductor regions 18.

Subsequently, an inter-layer insulator film 19 is formed on the whole surface of the substrate. The inter-layer insulator film 19 is constructed of a double-layer structure in which a silicon oxide film 19A deposited by CVD, and a silicon oxide film (BPSG) 19B deposited by CVD and capable of glass flow are stacked in succession.

The silicon oxide film 19A of the lower layer is formed in order to prevent B and P, contained in the silicon oxide film 19B, from leaking to the underlying element, and to ensure the dielectric strength of each part of the silicon oxide film 19B

thinned by the glass flow. The silicon oxide film 19A is formed at a thickness of, for example, about 500 - 2000 [Å].

The silicon oxide film 19B of the upper layer is formed in order to flatten the surface thereof for the purpose of enhancing the step coverage of overlying wiring (21). The silicon oxide film 19B is formed at a thickness of, for example, about 3000 - 7000 [Å].

Subsequently, the silicon oxide film 19B being the upper layer of the inter-layer insulator film 19 is subjected to the glass flow so as to flatten the surface thereof. By way of example, the glass flow is carried out in a nitrogen gas atmosphere at a high temperature of about 900 - 1000 [°C].

Subsequently, the part of the inter-layer insulator film 19 on each of the semiconductor regions 9, 17 and 18, the part thereof on the word line 7 (not shown) and the part thereof on the second electrode layer 15 (not shown) are selectively removed to form contact holes 19C. The contact holes 19C are formed by subjecting the upper part of the inter-layer insulator film 19 to wet etching, and the lower part thereof to anisotripic etching such as RIE. The contact hole 19C is in a tapered

shape in which the opening size of the upper side of the inter-layer insulator film 19C is large, and the opening size of the lower side thereof is small, so that the breaking of the overlying wiring (21) can be prevented. Alternatively, the contact holes 19C may well be formed by only the anisotropic etching.

Subsequently, a silicon oxide film 30 is formed on those parts of the silicon surfaces of the semiconductor regions 9, etc. which are exposed through the contact holes 19C. The silicon oxide film 30 is formed in order to prevent the B or P of the silicon oxide film 19B of the inter-layer insulator film 19 from being introduced into the principal surface parts of the semiconductor regions 9, etc. through the contact holes 19C by annealing at a later step (the drive-in diffusion of an impurity for forming semiconductor regions 20). In a case where the B has been introduced into the semiconductor regions 9 or 17 of the n-type or where the P has been introduced into the semiconductor regions 18 of the p-type, the effective impurity concentration of the semiconductor regions lowers, and the contact resistance between each semiconductor region and wiring connected thereto increases. The silicon oxide film 30 is

formed into a thin film whose thickness is about 120 - 300 [Å].

Subsequently, in the regions for forming the memory cell-selecting MISFET Q_s and the n-channel MISFET Q_n, the n-type impurity is introduced selectively into the principal surface parts of the semiconductor regions 9 and 17 through the contact holes 19C. The n-type impurity is passed through the silicon oxide film 30. This n-type impurity is subsequently subjected to the dirve-in diffusion, to form the n^+-type semiconductor regions 20 of high impurity concentration as shown in Fig. 24. The semiconductor region 20 is formed in order to prevent the situation that, in a case where the semiconductor region 9 or 17 and the contact hole 19C have not coincided due to a mask misregistration in the manufacturing process, the well region 2 and the wiring (21) to be passed through the contact hole 19C short-circuit. By way of example, the n-type impurity used for forming the semiconductor region 20 is As at a high impurity concentration on the order of 10^{15} [atoms/cm^2], and it is introduced by ion implantation at an energy level of about 110 - 130 [keV]. In the memory cell M, the semiconductor region 20 is made integral with the other semiconductor

region 9 of the MISFET Q_s, and it constructs a part of the source region or drain region. Since the semiconductor region 20 is formed by the ion implantation at the high impurity concentration, the contact resistance thereof with the complementary data line (21) can be lowered.

Subsequently, as illustrated in Fig. 25, there are formed the wiring leads 21 which are respectively connected with the semiconductor regions 9, 17, 18 etc. through the contact holes 19C and which extend on the inter-layer insulator film 19. The wiring leads 21 are formed by the step of forming the first layer of wiring, and they construct the complementary data lines 21, the Y-select signal lines 21, etc. as described before. The wiring 21 is constructed of a triple-layer structure in which a barrier metal film 21A, an aluminum film 21B and a protective film 21C are successively stacked. This wiring 21 is patterned by the use of anisotropic etching such as RIE.

The barrier metal film 21A is made of $MoSi_2$ deposited by sputtering, and is formed to a thickness of about 100 - 200 [Å]. Since the barrier metal film 21A is formed on the whole lower surface of the aluminum film 21B and can introduce Mo into

the aluminum film 21B, it can suppress the growth of the crystal grains of aluminum and mitigate stress migration.

The aluminum film 21B is doped with additives Cu and Si. It is deposited by sputtering, and is formed to a thickness of about 4000 - 6000 [Å].

The protective film 21C is made of $MoSi_x$ ($x = 0 < x < 1.2$), and is formed to a thickness of about 100 - 1000 [Å]. As described before, this protective film 21C is formed in order to protect the surface of the aluminum film 21B from a liquid which is used in the wet process for forming the wiring 21.

The respective layers of the wiring 21 are formed by a sputtering apparatus 50 shown in Fig. 29 (a schematic constructional view of a sputtering apparatus). As depicted in Fig. 29, the sputtering apparatus 50 is mainly configured of a single-loader chamber 51, a twin-loader chamber 52, a cleaning chamber 53 and a sputtering chamber 54.

The single-loader chamber 51 is so constructed that a plurality of wafers 55A accommodated in a cassette 55 are successively supplied into the cleaning chamber 53 and the sputtering chamber 54 through wafer conveyance belts 56. The cassette

55 is so constructed that the plurality of wafers 55A can be held in erected states. The cassette 55 is transported to a feed position for the wafer 55A by an elevator unit 51A. At this position, the cassette is erected so that the plane of the wafer 55A and the conveyance direction thereof may coincide to permit the smooth feed of the wafer 55A. When continuous processing is performed, the single-loader chamber 51 is used conjointly with the twin-loader chamber 52.

The twin-loader chamber 52 is so constructed that wafers 55A can be supplied into the cleaning chamber 53 and the sputtering chamber 54, and that processed wafers 55A can be received therein. Although not shown, a cassette 55 in which the wafers 55A to be supplied are accommodated is constructed so as to be transported by an elevator unit 52A. A cassette 55 in which the processed wafers 55A are accommodated is constructed so as to be transported by an elevator unit 52B.

The cleaning chamber 53 is so constructed that the wafer 55A conveyed from the twin-loader chamber 52 by the wafer conveyance belt 56 is held and rotated in the direction of arrows by a quartz arm 53A. The quartz arms 53A are arranged in

a number of four at equal intervals of 90 degrees, and the four quartz arms 53A are constructed so as to rotate about an identical axis of rotation. The wafer 55A held by the quartz arm 53A confronts a sputter-etching electrode 53B and has its surface cleaned, or it is heated by a pre-processing heater 53C. In addition, the quartz arm 53A is constructed so as to hold the processed wafer 55A conveyed from the sputtering chamber 54 by the wafer conveyance belt 56, and to transport it into the twin-loader chamber 52.

The sputtering chamber 54 is provided with a wafer holder 54A which can hold the wafer 55A in the erected state. Likewise to the quartz arms 53A, the wafer holders 54A are arranged in a number of four at equal intervals of 90 degrees, and the four wafer holders 54A are constructed so as to rotate about an identical axis of rotation. Sputtering portions 54I, 54II and 54 III are respectively disposed at positions which confront the surfaces (planes for holding the wafers 55A) of the three wafer holders 54A other than the wafer holder 54A located at the wafer conveyance belt 56. A heater 54B is arranged on the rear side of each of the three wafer holders 54A.

Each of the sputtering portions 54I, 54II and 54III is provided with a shield plate 54C, a shutter 54D, a target case 54E, a target 54F, a magnet 54G and a target rotating unit 54H in this order as viewed from the side of the wafer holder 54A. The target 54 of the sputtering portion 54I is made of $MoSi_2$. The target 54 of the sputtering portion 54II is made of Al-Cu-Si. The target 54F of the sputtering protion 54III is made of $MoSi_x$. Thus, the sputtering chamber 54 can successively and continuously stack the barrier metal film 21A, aluminum film 21B and protective film 21C on the wafer 55A, namely, on the inter-layer insulator film 19 of the DRAM within an identical vacuum system (identical chamber).

In a DRAM wherein the protective film 21C (the metal wiring of the upper layer) is stacked directly on the aluminum film 21B (the metal wiring of the lower layer) of the wiring 21, the aluminum film 21B is formed by sputtering within the vacuum system, and thereafter, the protective film 21C is continuously formed on the aluminum film 21B by sputtering within the same vacuum system, whereby the production of an aluminum oxide on the surface of the aluminum film 21B can be mitigated, so that

the specific resistance of the wiring 21 which is formed of the aluminum film 21B and the protective film 21C can be lowered. The lowering of the specific resistance of the wiring 21 can raise the operating speed of the DRAM.

In addition, with the wiring 21 which is mainly made of the aluminum film 21B doped with an element (such as Cu) for reducing migration, the aluminum film 21B doped with the element is formed, this aluminum film 21B is overlaid with the protective film 21C for protecting it from a liquid which is used in a wet process, an etching mask (which is not shown and which is an etching mask for the wiring 21) is formed on this protective film 21C, the protective film 21C and the aluminum film 21B are etched into a predetermined shape by the use of this etching mask, and the wet process for removing the etching mask is thereafter performed, whereby the reaction of a cell which is constructed of the aluminum film 21B and an intermetallic compound formed by the aluminum and the element of this film can be prevented during the etching or wet process, so that the damages of the aluminum film 21 attributed to the galvanic reaction can be prevented. As a result, the wiring 21 can have inferior shapes

decreased, breaking prevented or the migration reduced.

After the step of forming the wiring 21 illustrated in Fig. 25, an inter-layer insulator film 22 is formed on the whole surface of the substrate including the wiring 21. As stated before, the inter-layer insulator film 22 is constructed of a triple-layer structure.

A silicon oxide film 22A as the lower layer is formed at a thickness of about 1000 - 2000 [Å].

A silicon oxide film 22B as the middle layer is formed in order to flatten the surface thereof. The silicon oxide film 22B is formed by several times (2 - 5 times) of coating (coating to a total thickness of about 1000 - 2000 [Å]) and a baking treatment (at about 450 [°C]), into a densified film. Alternatively, the silicon oxide film 22B may well be formed by gradually heightening the temperature of a baking treatment, into a film of good quality.

A silicon oxide film 22C as the upper layer is formed in order to raise the strength of the whole inter-layer insulator film 22. The silicon oxide film 22C is formed at a thickness of about 4000 - 7000 [Å].

Subsequently, as illustrated in Fig. 26, a contact hole 22D is formed in the inter-layer insulator film 22. The contact hole 22D is formed into a stair shape in vertical section by a resist retraction method which employs a multilayer photoresist film (etching mask) and anisotropic etching such as RIE. Thereafter, annealing at about 400 [°C] is performed in order to remedy damages ascribable to the etching.

Subsequently, as illustrated in Figs. 2 and 3, wiring 23 which extends on the inter-layer insulator film 22 and which is formed by the step of forming the second layer of wiring is formed so as to connect to the wiring 21 through the contact hole 22D. As stated before, the wiring 23 is constructed of a double-layer structure in which an underlying film 23A and an aluminum film 23B are successively stacked.

The underlying film 23A of the lower layer is formed of $MoSi_2$ deposited by sputtering, and to a thickness of about 100 - 1000 [Å].

The aluminum film 23B of the upper layer is deposited by sputtering, and it is formed to a thickness of about 7000 - 12000 [Å] greater than the thickness of the aluminum film 21B of the wiring

21. Likewise to the aluminum film 21B, the aluminum film 23B is doped with both Cu and Si in equal amounts.

In this manner, the protective film 21C (refractory metal silicide film, which is of $MoSi_x$ in the present embodiment) having a silicon content greater than 0 and less than 2 (the optimum value being greater than 0 and at most 1.2) is interposed between that aluminum film 21B of the wiring 21 which is doped with the element (Cu) for reducing migration and that aluminum film 23B of the wiring 23 which is connected to the aluminum film 21B through the contact hole 22D formed in the inter-layer insulator film 22, whereby the grains of the aluminum film 21B of the wiring 21 can be prevented from precipitating at the boundary of the protective film 21C and the aluminum film 23B through the protective film 21C and forming an aluminum oxide, so that the contact resistance between the aluminum film 21B and the aluminum film 23B can be lowered. As a result, the available percentage concerning the connected parts of the wiring 21 and the wiring 23 can be heightened.

Moreover, since the contact resistance between the wiring 21 and 23 can be lowered, the speed

of signal transmission can be raised, and the operating speed of the DRAM can be heightened.

After the step of forming the wiring 23, annealing is carried out in order to remedy damages ascribable to etching (anisotropic etching) for forming the wiring 23.

Subsequently, a passivation film not shown is formed on the whole surface of the substrate including the wiring 23.

The DRAM of the present embodiment is substantially finished up by performing these series of steps.

Although, in the above, the inventions made by the inventors have been concretely described in conjunction with the embodiment, it is a matter of course that the present invention is not restricted to the foregoing embodiment, but that it can be variously altered within a scope not departing from the purport thereof.

[Effects of the Invention]

The effects obtainable from the representatives of the invention disclosed hereinbefore will be summarized in the following.

It is possible to improve the breakdown strength of the dielectric film and accordingly the electric reliability of the semiconductor integrated circuit device including a DRAM having a memory cell constructed of an information storing capacitive element of stacked structure.

It is also possible to reduce the number of steps of fabricating the semiconductor integrated circuit device having the DRAM.

4. Brief Description of the Drawings

Fig. 1 is an equivalent circuit diagram showing the principal portion of the DRAM according to one embodiment of the present invention;

Fig. 2 is a top plan view showing the principal portion of the memory cell array of the DRAM;

Fig. 3 is a section showing the principal portion of the memory cell array and peripheral circuit of the DRAM;

Figs. 4 and 5 are top plan views showing the principal portion of the memory cell array at predetermined fabrication steps;

Figs. 6 to 8 are diagrams plotting the data which are measured by the Auger electronic spectroscopy from the components of a wiring used in the DRAM;

Figs. 9 to 26 are sections showing the principal portions of the memory cell array and peripheral circuits of the DRAM at individual fabrication steps;

Fig. 27 is a diagram plotting the impurity atom concentration profile of a channel stopper region for separating the individual elements of the DRAM;

Fig. 28 is a diagram plotting the oxidation characteristics of a silicon nitride film constituting the dielectric film of the information storing capacitive element of the DRAM; and

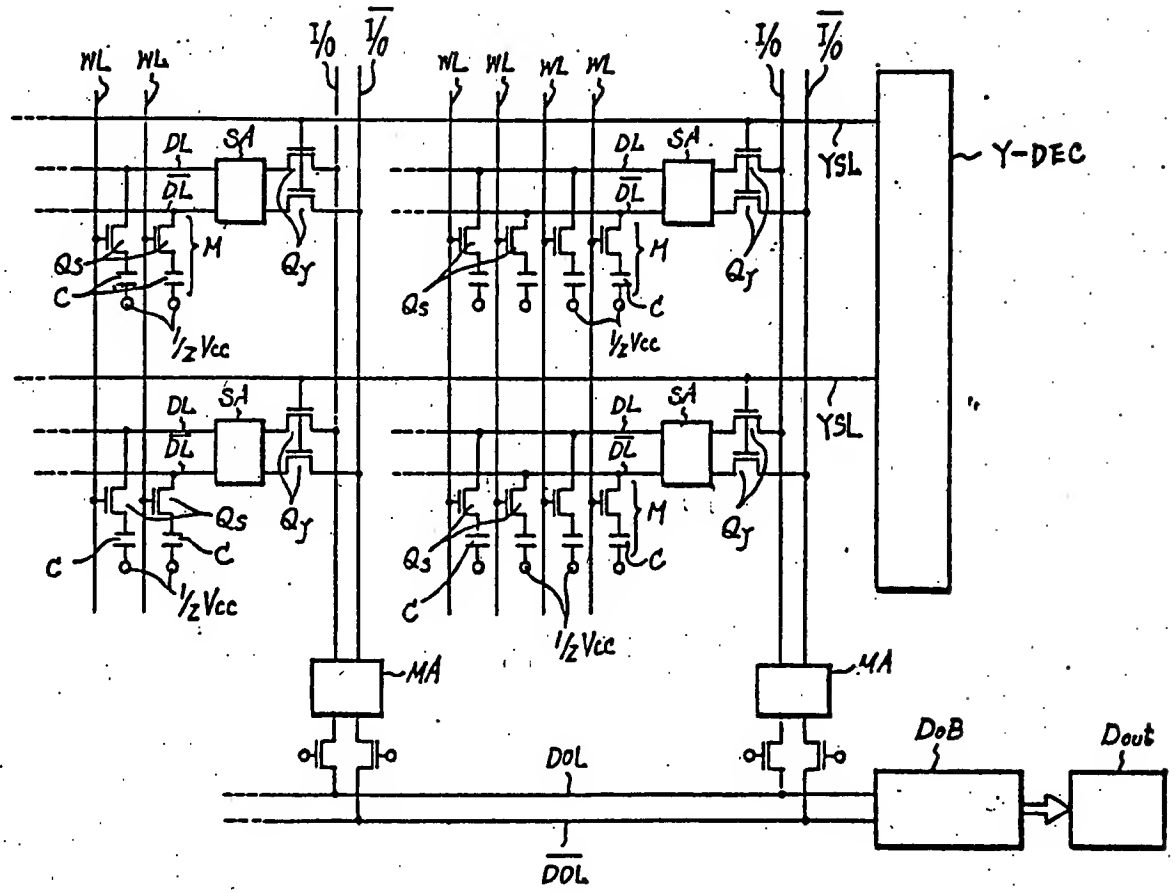
Fig. 29 is a schematic view showing a sputtering apparatus for forming a wiring to be used in the DRAM.

In the Drawings: M...Memory Cell; Qs...Memory Cell Selecting MISFET; Qn and Qp...MISFETs; C...Information Storing Capacitive Element; WL...Word Line; DL...Complementary Data Line; YSL...Y-Select Signal Line; 4A...Channel Stopper Region; 4B...Potential Barrier Layer; 7...Gate Electrode or Word Line; 9, 10, 13A, 17, 18 and 20... Semiconductor Regions; 12...Interlayer Insulating

Film; 12A...Connection Hole; 13...First Electrode Layer; 14...Dielectric Film; 14A...Silicon Nitride Film; 14B...Silicon Oxide Film; 15...Second Electrode Layer; 21 and 23...Wirings; 21A...Barrier Metal Film; 21B and 23B...Aluminum Films; 21C...Passivation Film; 23A...Base Film; and 50...Sputtering Apparatus.

Agent: Shuki AKITA, Patent Attorney

FIG. 1



Agent, Patent Attorney, Shuki AKITA

FIG. 2

第３図

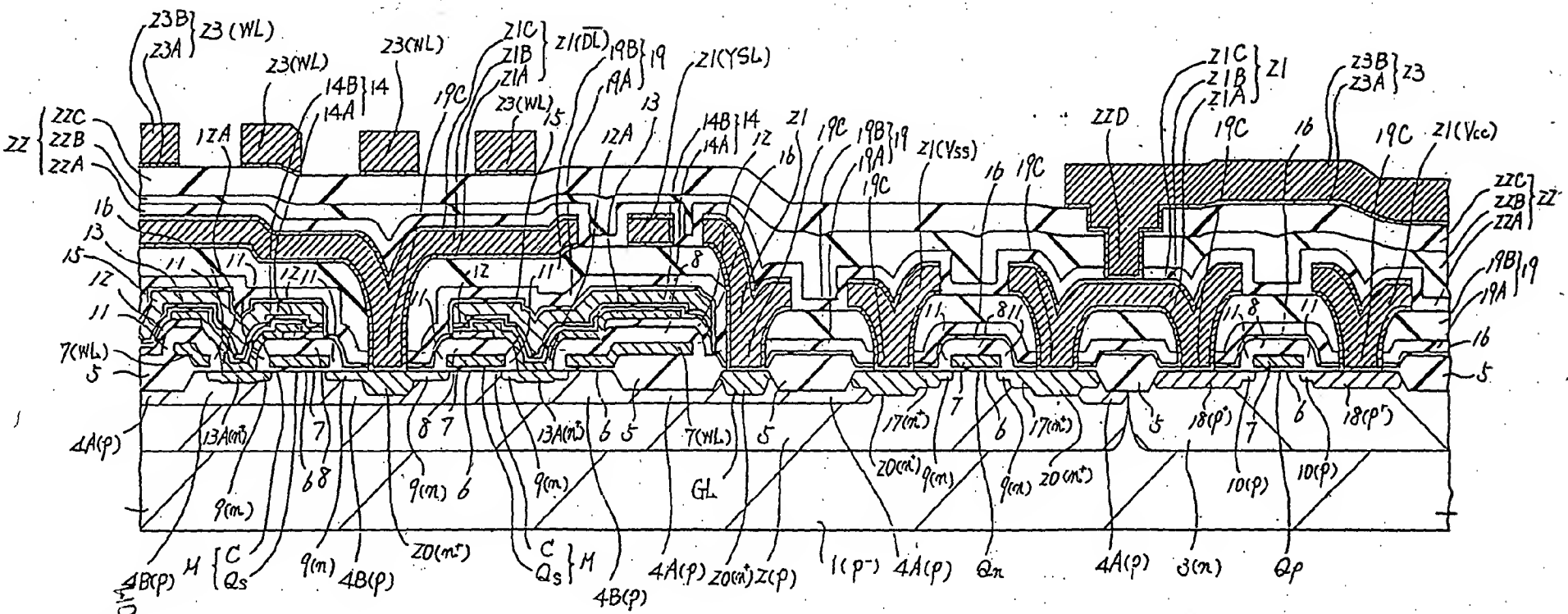
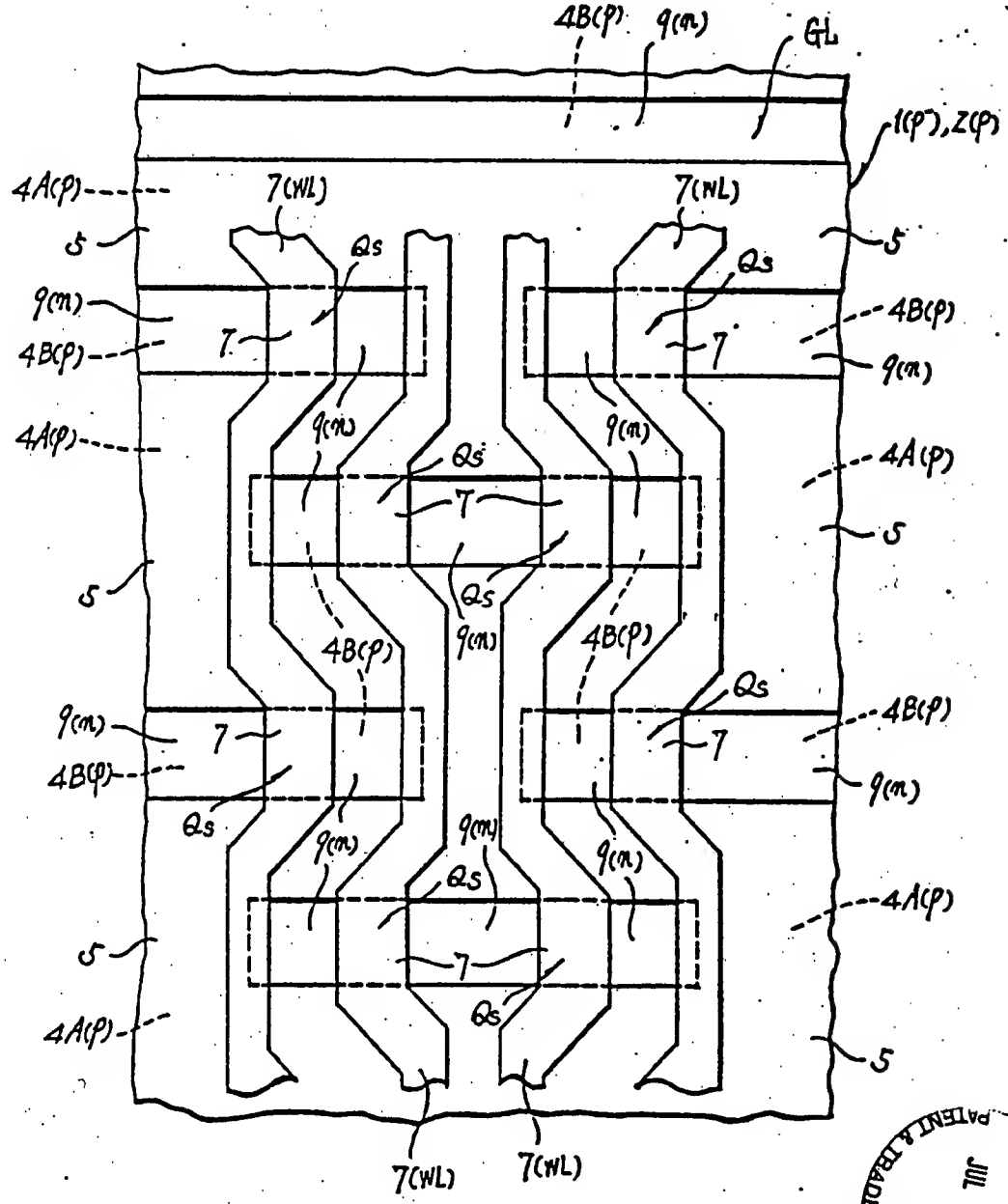


FIG. 4



第5図

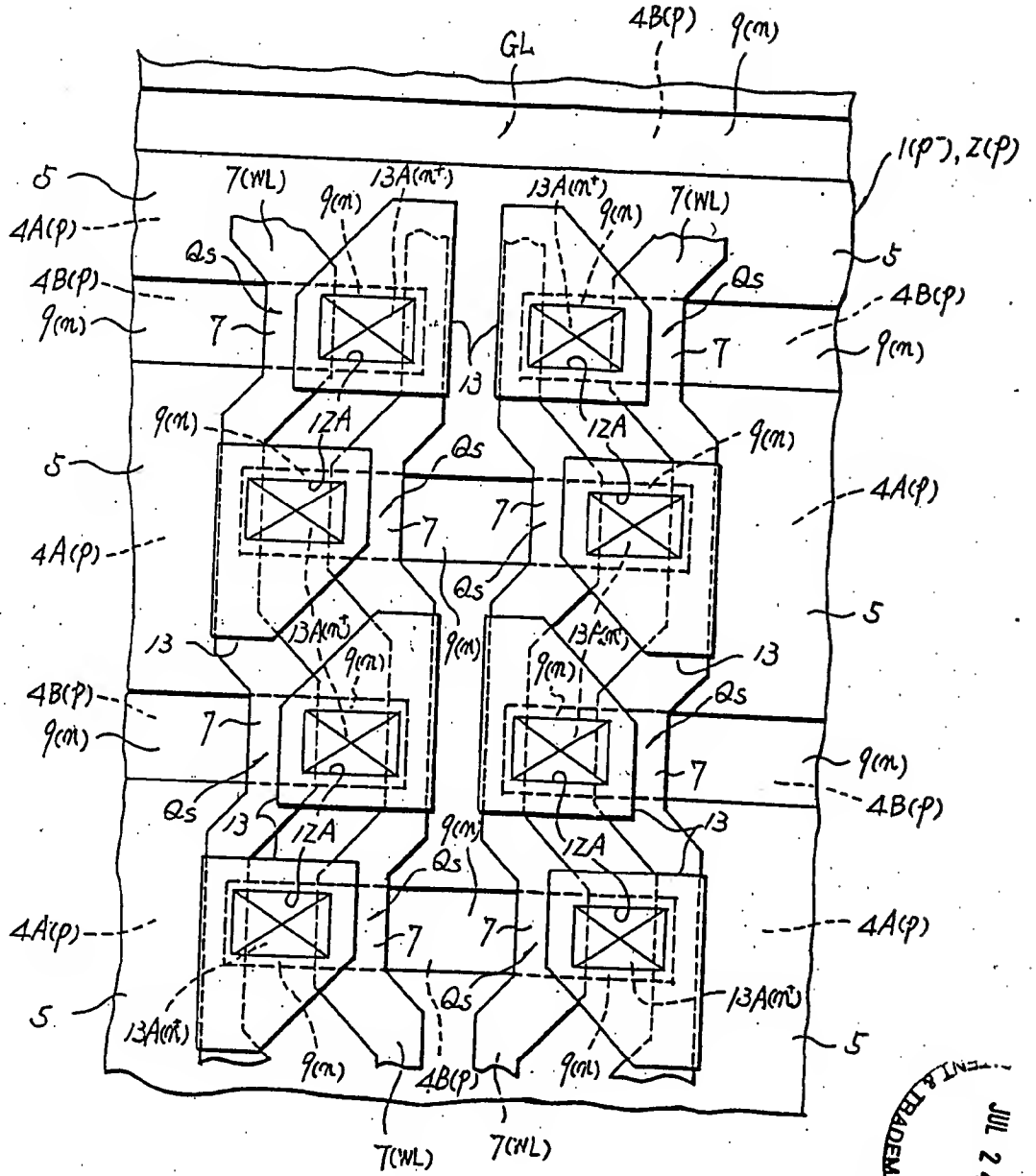


FIG. 6

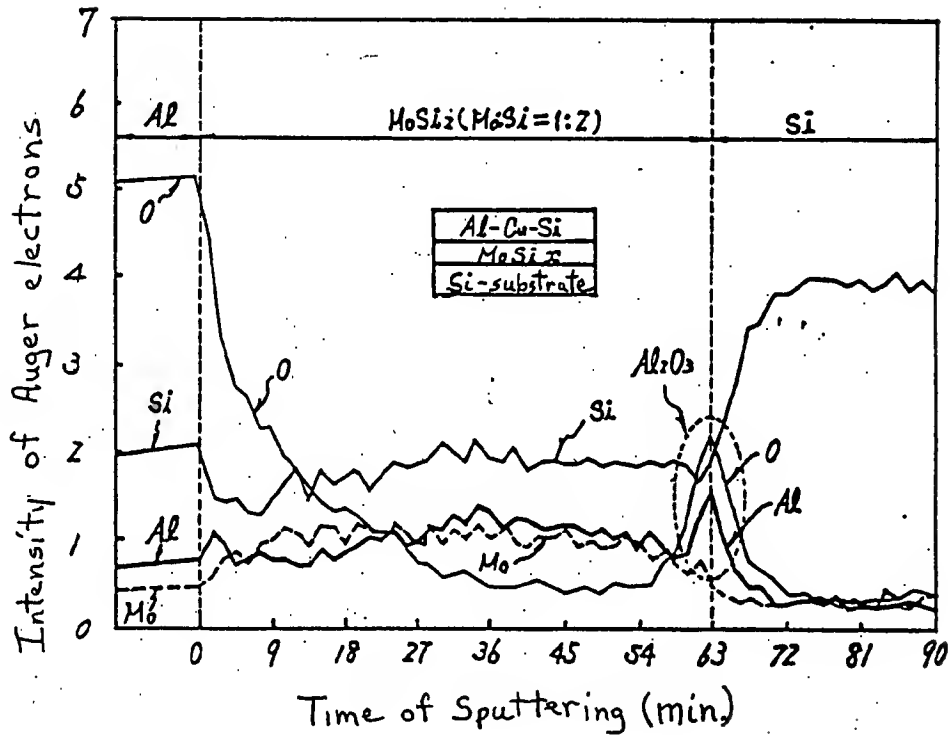


FIG. 7

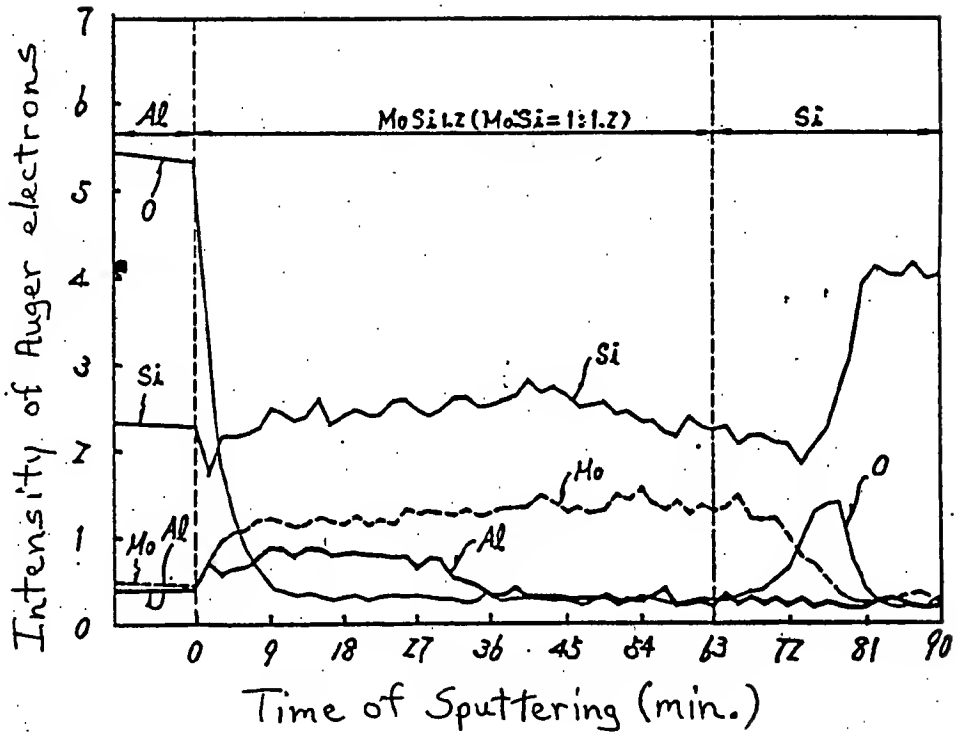


FIG. 8

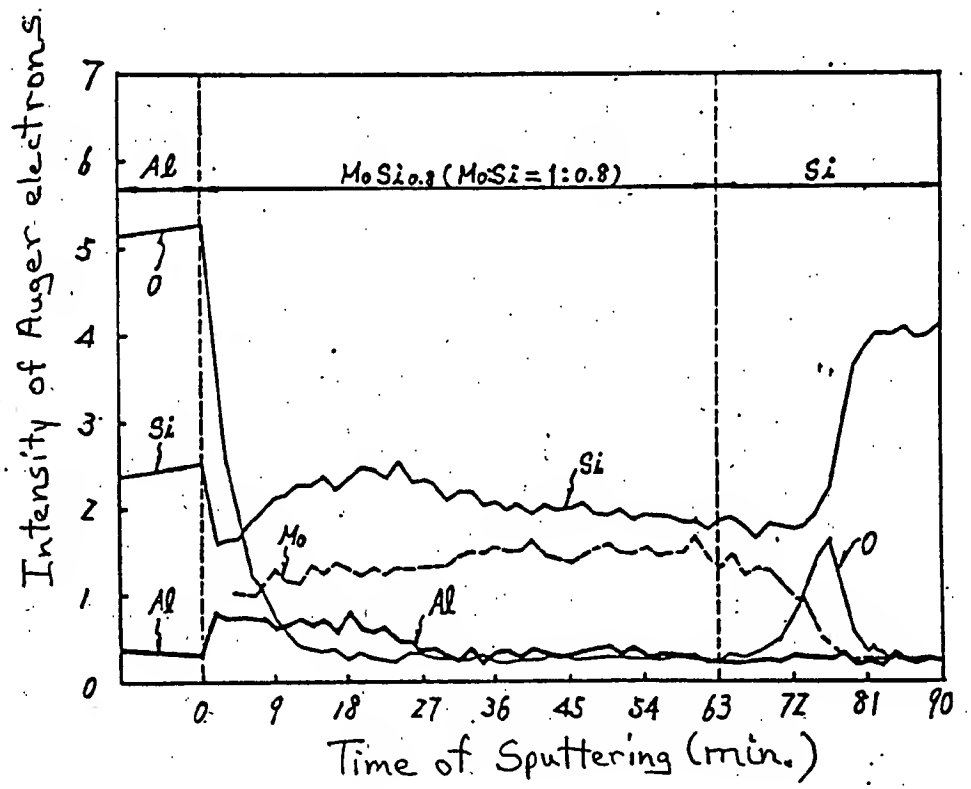


FIG. 9

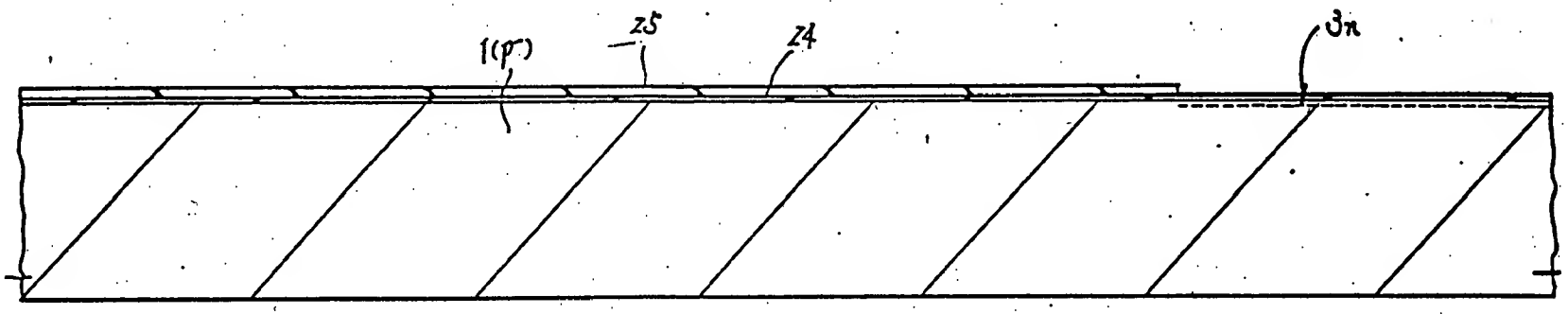


FIG. 10

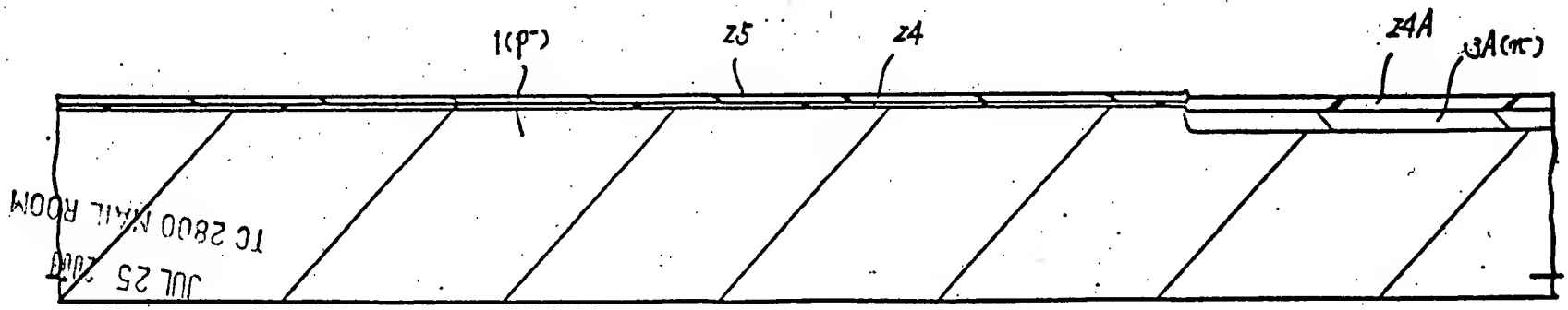


FIG. 11

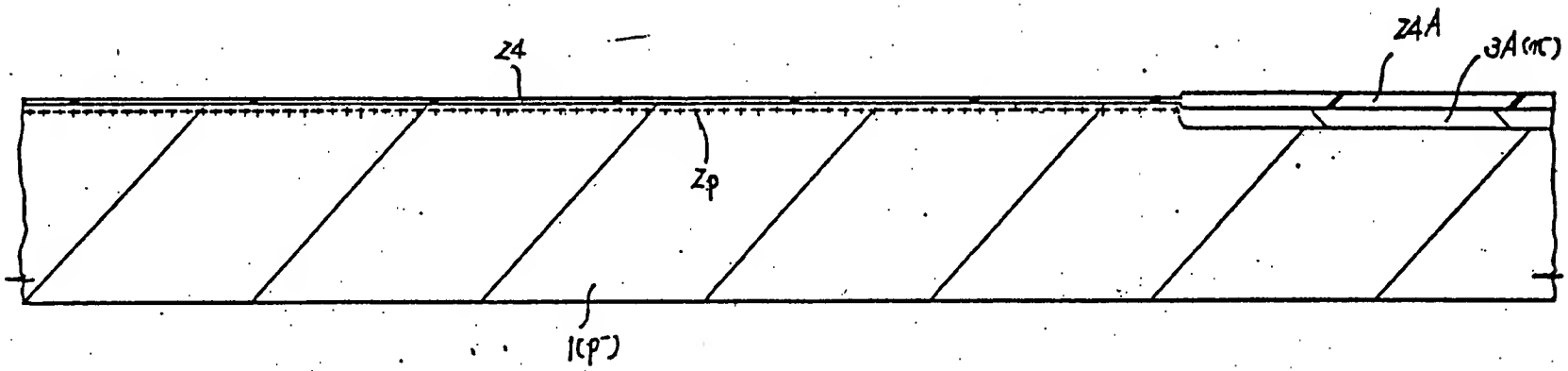


FIG. 12

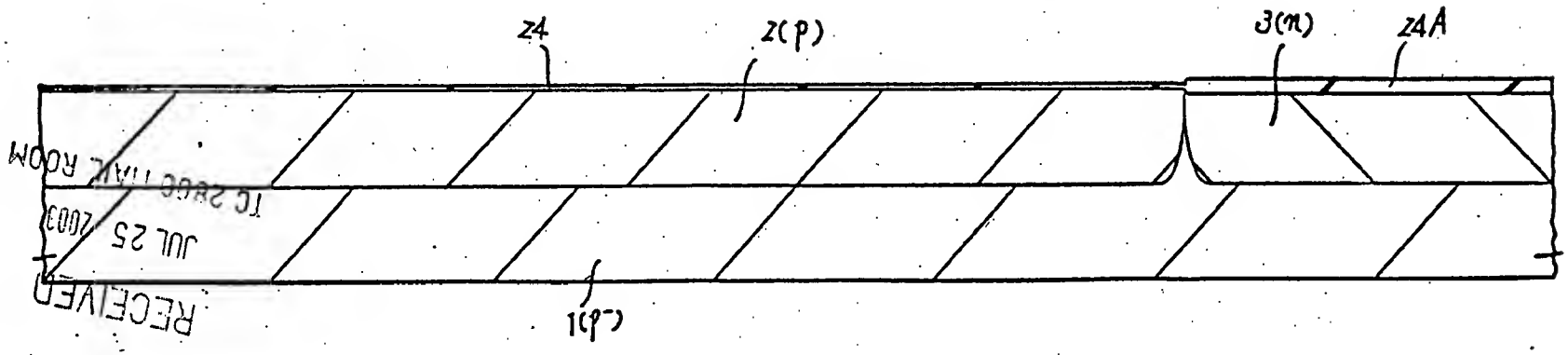


FIG. 13

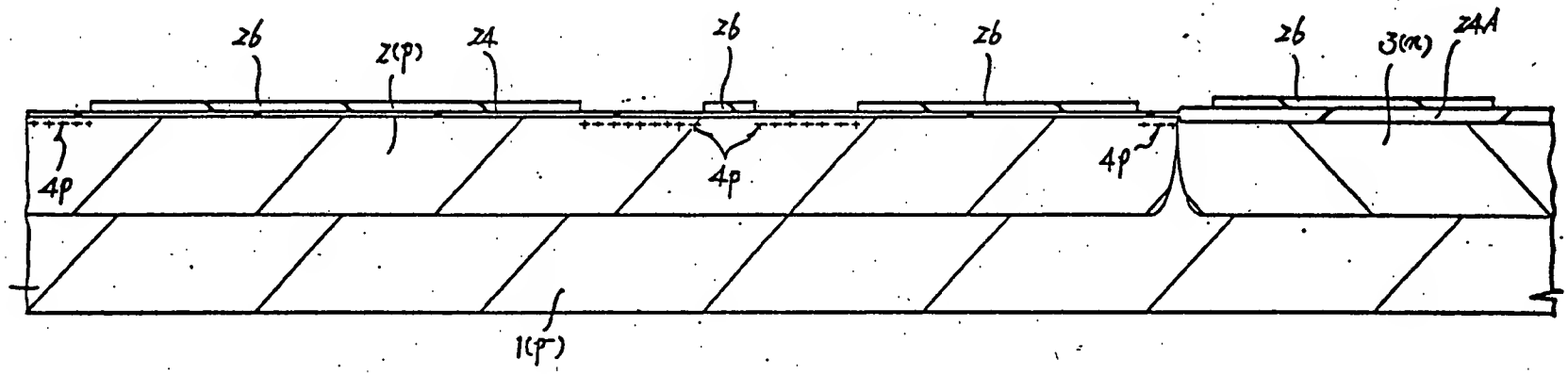


FIG. 14

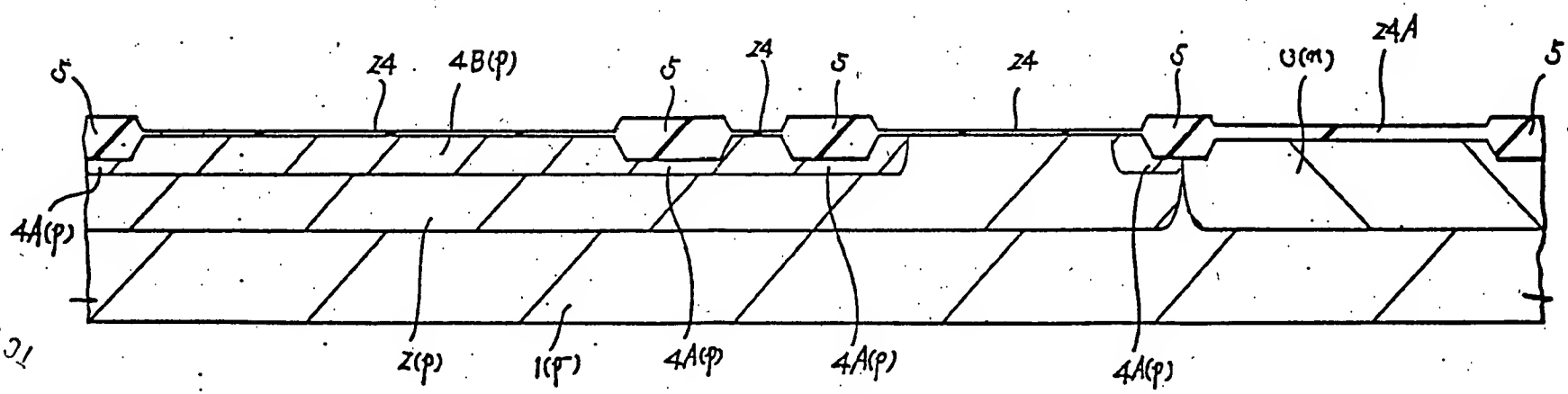


FIG. 15

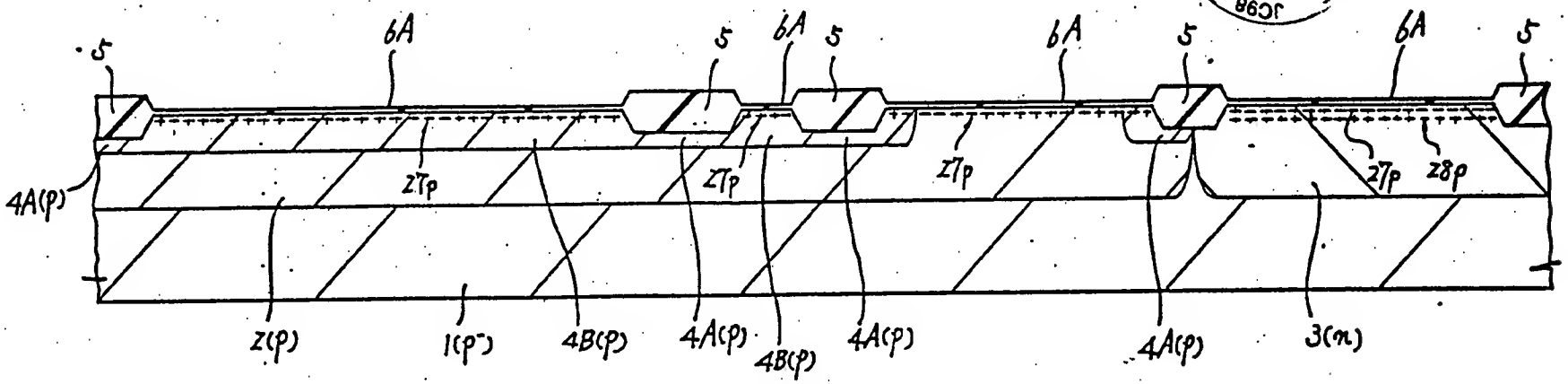


FIG. 16

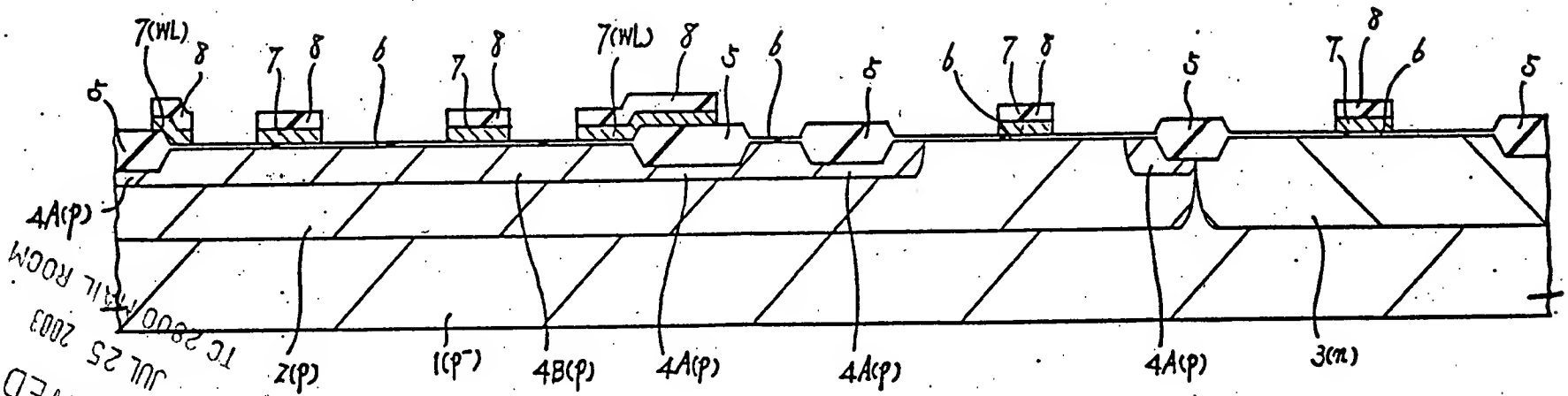


FIG. 17

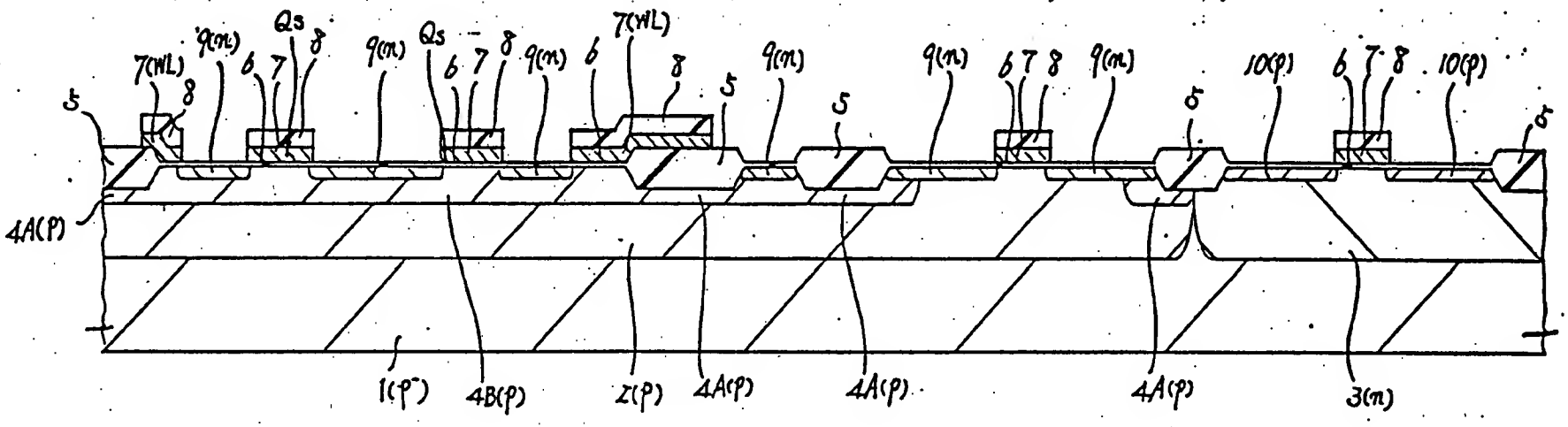


FIG. 18

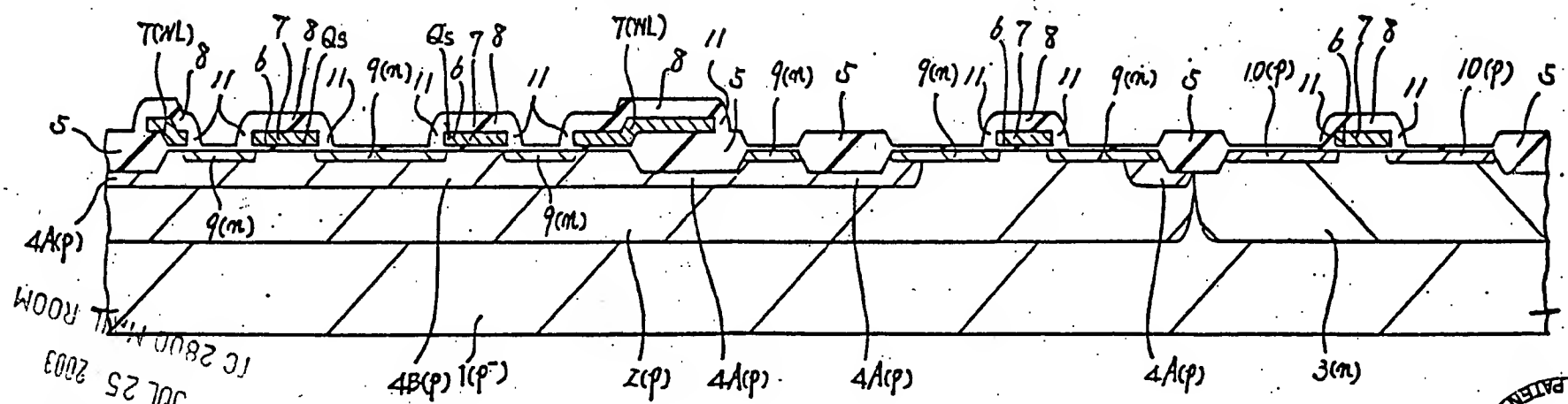


FIG. 19

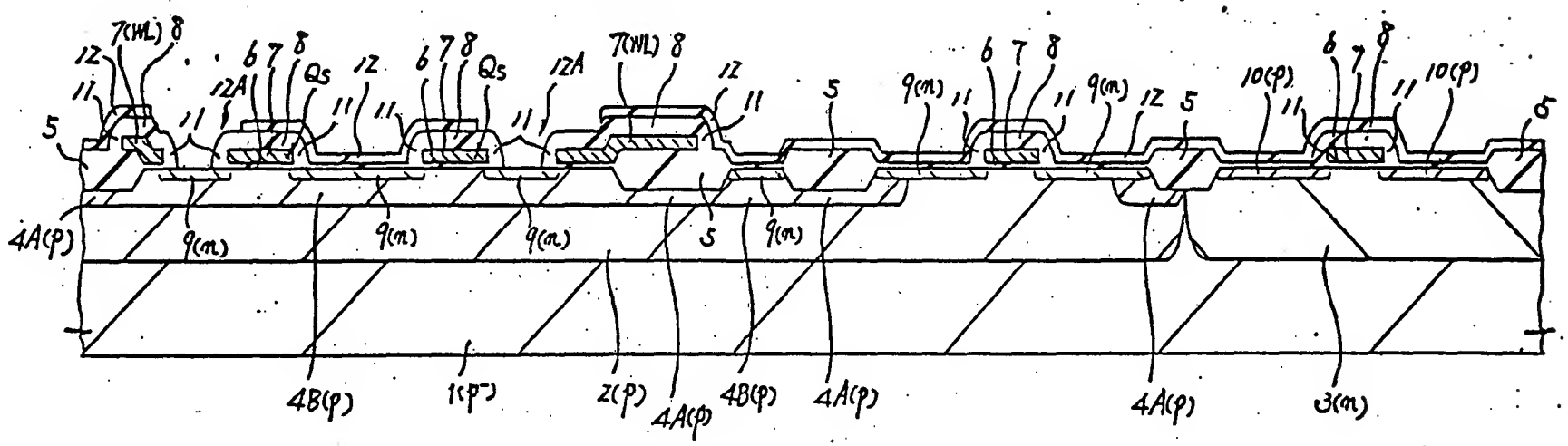


FIG. 20

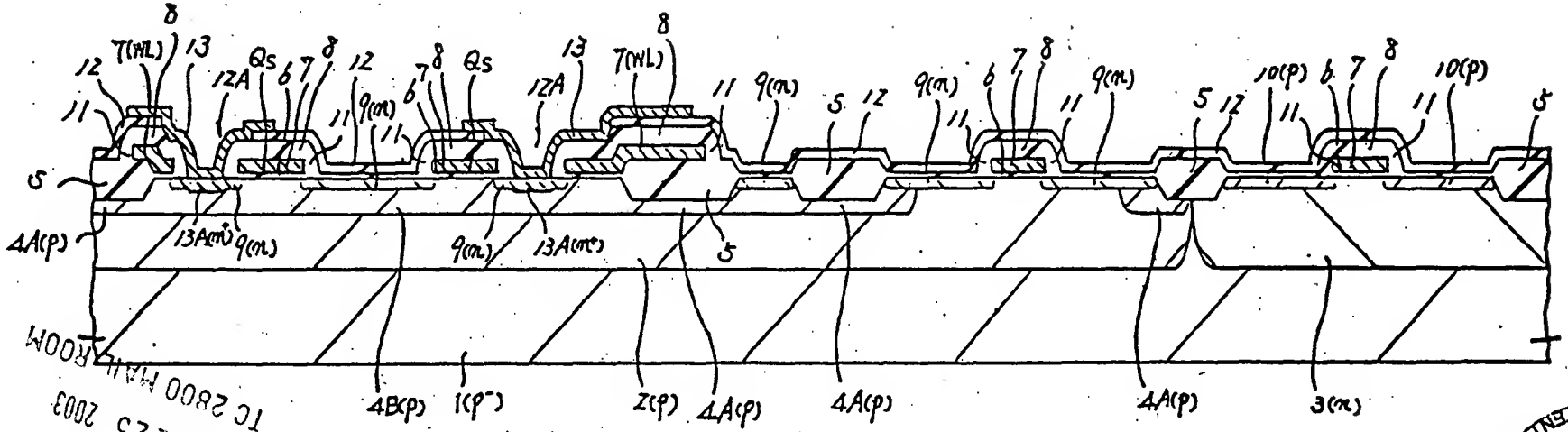


FIG. 21

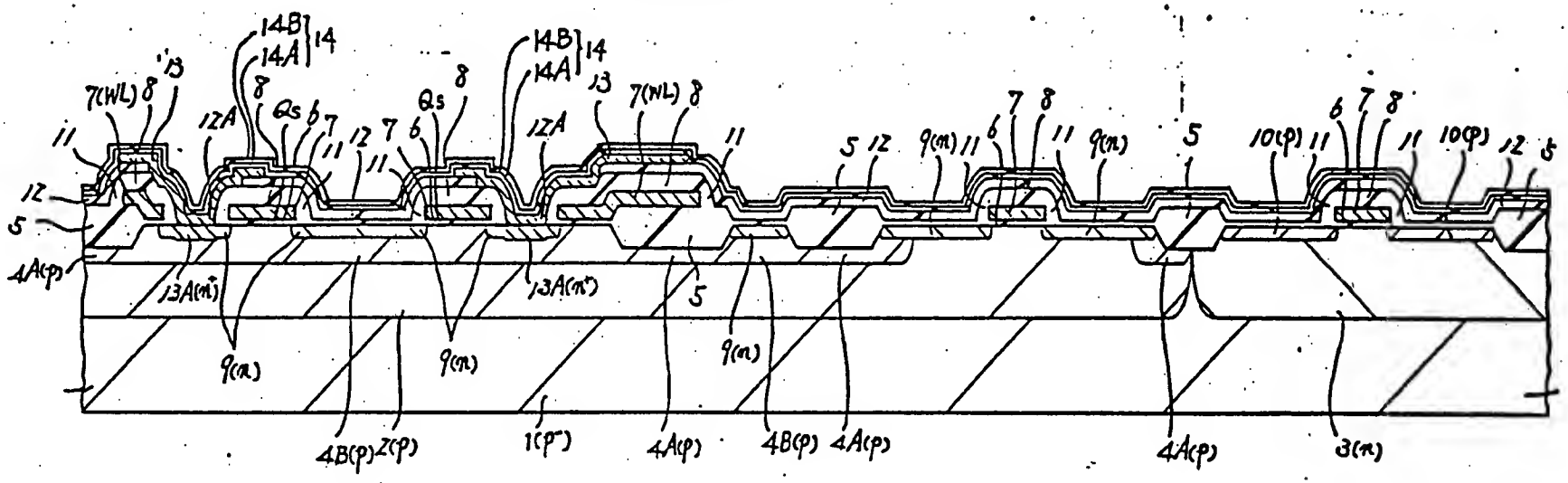


FIG. 22

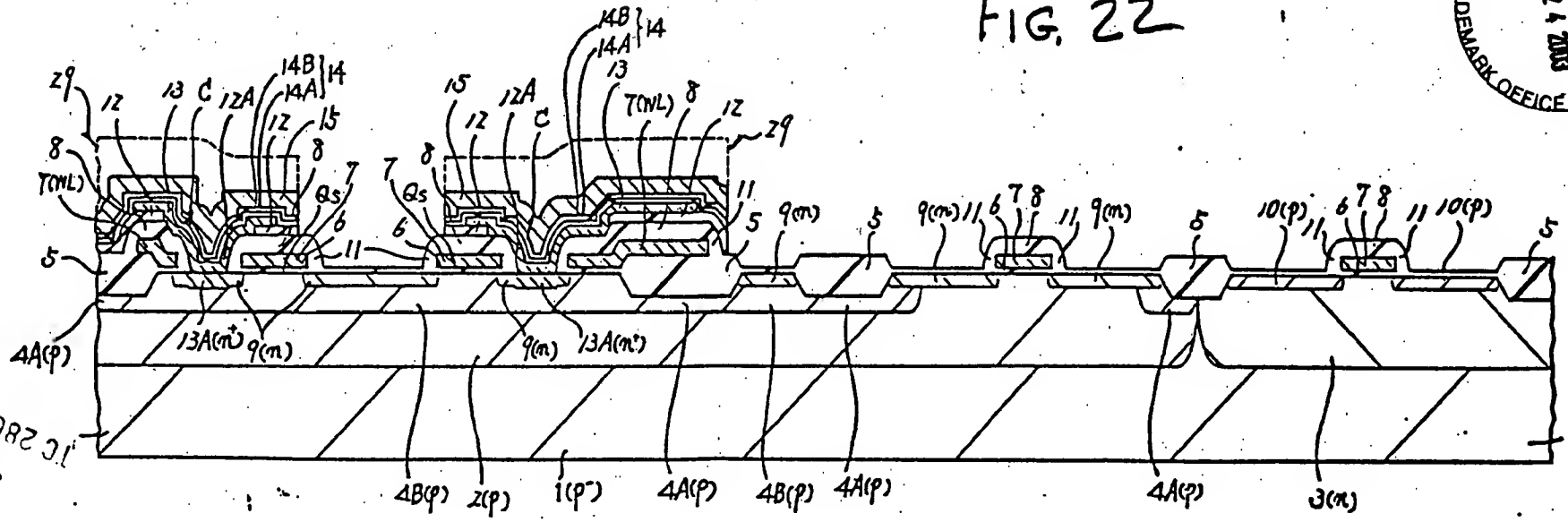


FIG. 23

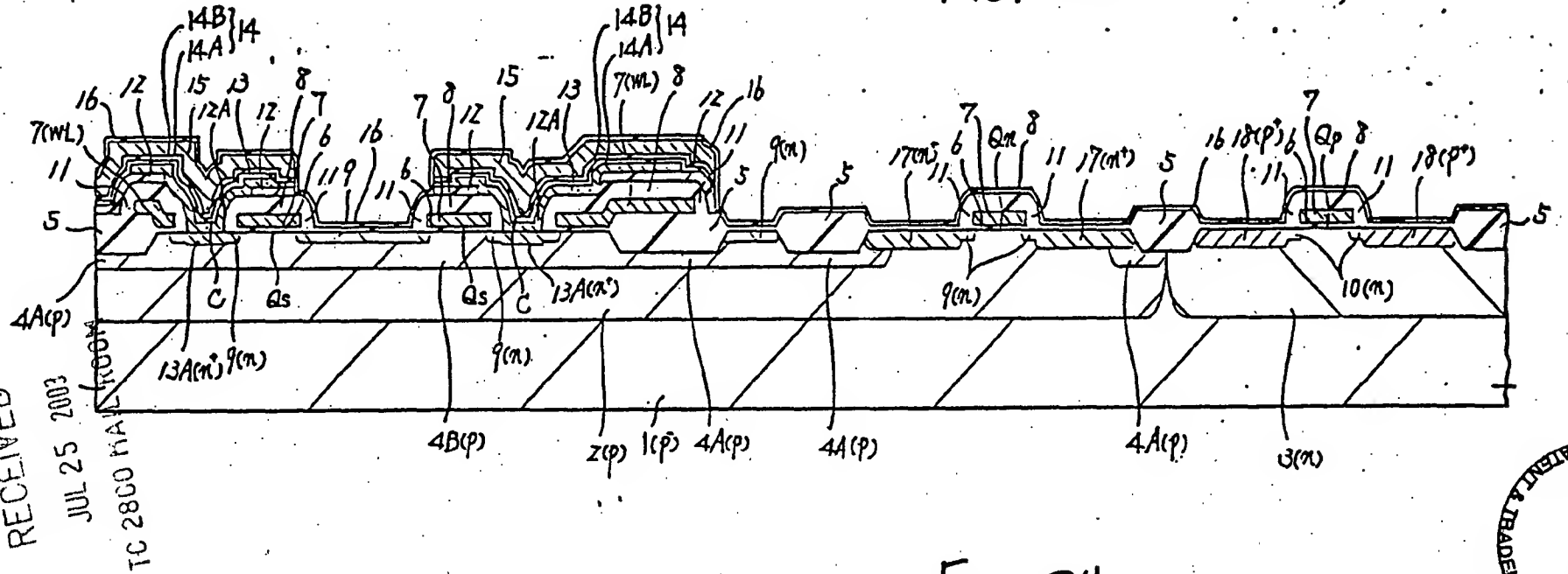


FIG. 24

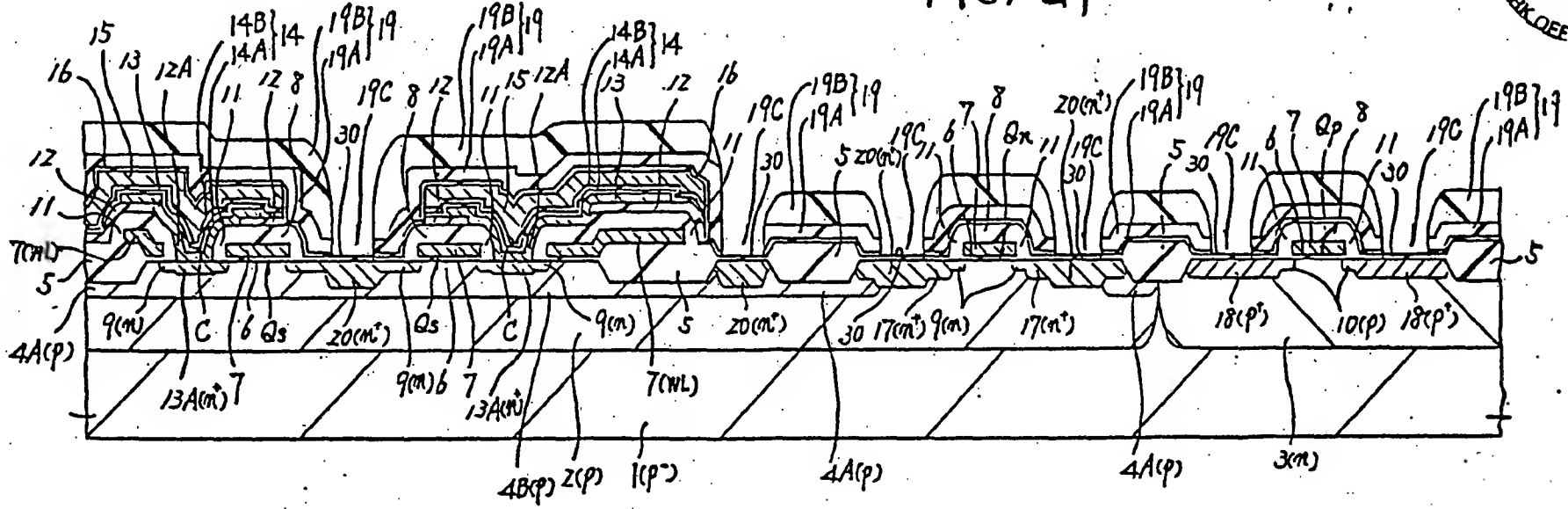


FIG. 25

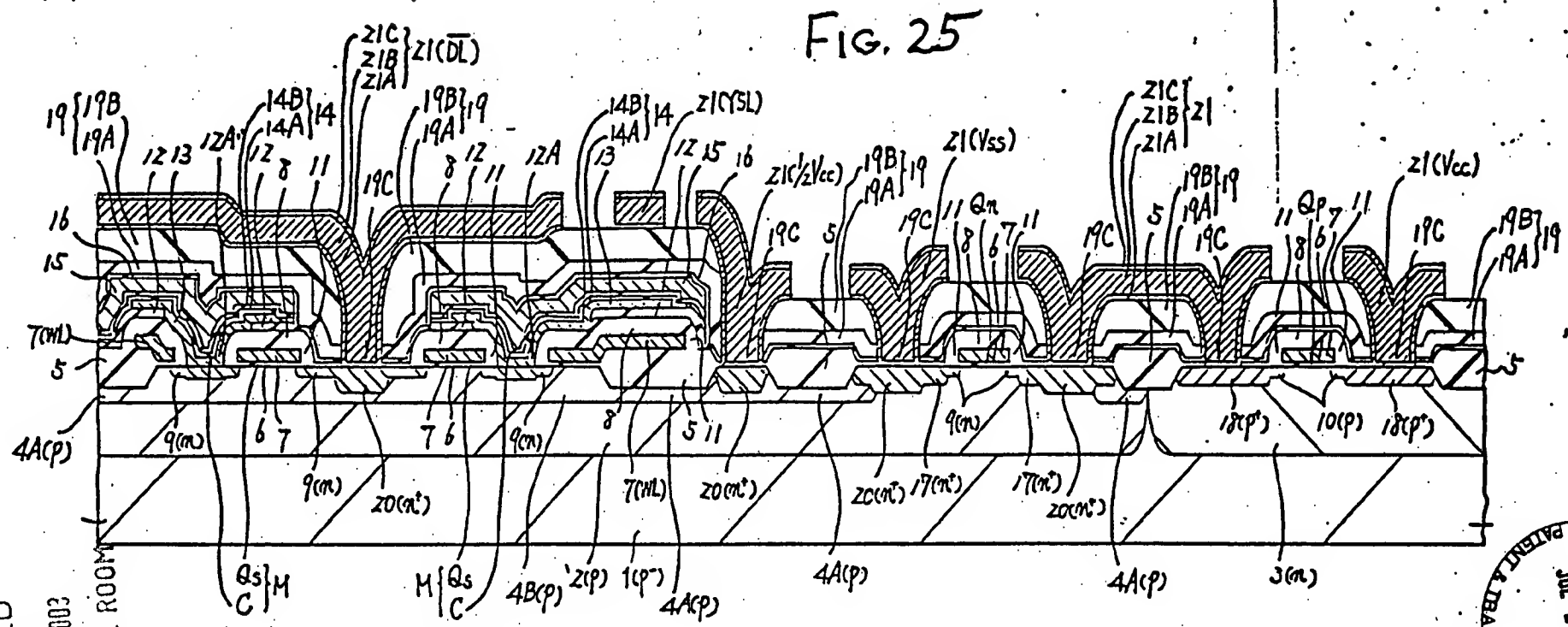


FIG. 26

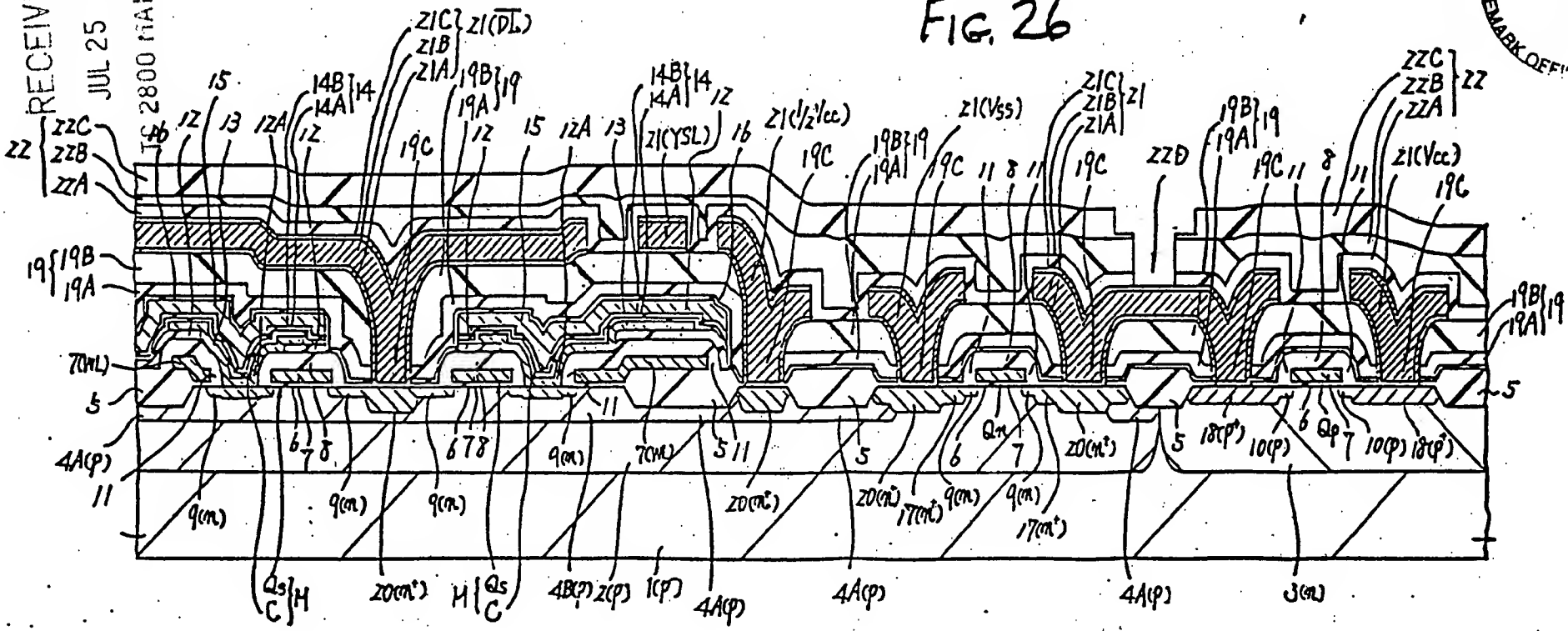


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FIG. 27

FIG. 28

FIG. 29